CMR ENGINEERING COLLEGE
UGC AUTONOMOUS
(Approved by AICTE - New Delhi. Affiliated to JNTUH and Accredited by NAAC & NBA)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE FILE

ON

FPGA PROGRAMMING

III B.TECH II SEM

AY 2022-23

CONTENTS:

1. Department Vision & Mission

Vision:

- To promote Excellence in Technical Education and Scientific Research in Electronics and Communication Engineering for the benefit of Society.

Mission:

- To impart Excellent Technical Education with State of Art Facilities inculcating Values and lifelong learning attitude.
- To develop Core Competence in our students imbibing Professional Ethics and Team Spirit.
- To encourage Research benefiting Society through Higher Learning.

2. List of PEO's, PO's & PSO's

PROGRAM EDUCATIONAL OBJECTIVES (PEO's):

PEO 1: Establish themselves as successful professionals in their career and higher education in the field of Electronics & Communication Engineering and allied domains through rigorous quality education.

PEO 2: Develop Professionalism, Ethical values, Excellent Leadership qualities, Communication Skills and teamwork in their Professional front and adapt to current trends by engaging in lifelong learning.

PEO 3: Apply the acquired knowledge & skills to develop novel technology and products for solving real life problems those are economically feasible and socially relevant.

PEO 4: To prepare the graduates for developing administrative acumen, to adapt diversified and multidisciplinary platforms to compete globally.

PROGRAM OUTCOMES (PO's):

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES(PSO's):

1. Ability to apply concepts of Electronics & Communication Engineering to associated research areas of electronics, communication, signal processing, VLSI, Embedded systems, IoT and allied technologies.
2. Ability to design, analyze and simulate a variety of Electronics & Communication functional elements using hardware and software tools along with analytic skills.

3. Mapping of course outcomes with PO's

Course Outcomes:

Upon completion of the course, students will be able to:

1. Explain the Architecture of SPLD's, CPLD's and FPGA's.
2. Analyze the Universal Design Methodology for Programmable Devices.
3. Design Digital circuits using Data flow and Behavioral Descriptions.
4. Design Digital circuits using Structural and Switch level Descriptions.
5. Analyze mixed type descriptions, Procedures, Tasks and understand about formal verification.

Mapping of CO's with PO's:

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2	2	2	-	-	-	-	3	3	3
CO2	3	3	2	2	3	-	-	-	-	3	3	3
CO3	3	3	3	2	3	-	-	-	-	3	3	3
CO4	3	3	3	3	3	-	-	-	-	3	3	3
CO5	3	3	3	3	3	-	-	-	-	3	3	3
AVG	3	3	3	3	3	-	-	-	-	3	3	3

CO's/ PSO's	PSO1	PSO2
CO1	3	3
CO2	3	3
CO3	3	3
CO4	3	3
CO5	3	3
AVG	3	3

4. Syllabus

UNIT-I

Simple Programmable Logic Devices (SPLD's):

Programmable Read Only Memories (PROMs), Programmable Logic Arrays (PLAs), Programmable Array Logic (PALs), the Masked Gate Array ASIC.

Complex Programmable Logic Devices (CPLD's):

CPLD Architectures, Function Blocks, I/O Blocks, Clock Drivers, Interconnect CPLD Technology and Programmable Elements, Embedded Devices.

Field Programmable Gate Arrays (FPGA's):

FPGA Architectures, Configurable Logic Blocks, Configurable I/o Blocks, Embedded Devices, Programmable Inter Connect, Clock Circuitry, SRAM vs. Anti-fuse programming, FPGA Selection Criteria.

UNIT – II

Universal Design Methodology for Programmable Devices:

Introduction to UDM and UDM-PD, writing a Specification, Specification Review, Choosing Device and Tools, Design, Verification, Final Review, System Integration and Test. Hardware Descriptive Languages, Structure of VHDL & Verilog module, operator, Data types, Top-Down Design, Synchronous Design, Floating Nodes, Bus Contention, One-Hot state Encoding.

UNIT –III

Data flow Description and Behavioral Descriptions:

Introduction to styles types of hardware description –Behavioral, Structural, Dataflow and Mixed type and language descriptions.

Data flow Description: Structure of the dataflow description, Signal Declaration and Assignment Statements, Concurrent Signal assignments, Constant declaration and assignments, assigning a delay time to the signal, Data type-Vectors.

Behavioral Descriptions: Structure of the HDL Behavioral description, The VHDL/ Verilog HDL variable – assignment statement, sequential statement – IF, signal and variable assignment, CASE & LOOP statements.

UNIT –IV

Structural and Switch level Descriptions:

Structural Description: Organization of the structural description, binding, state machines, Generate (HDL), Generic (VHDL), and parameter (Verilog).

Switch level Description: Useful definitions, Single NMOS & PMOS switches-verilog & VHDL description of NMOS & PMOS Switches, serial and parallel combinations of switches, Switch level Description of –primitive gates, Simple combinational logics, simple sequential circuits, Bidirectional switches.

UNIT – V

Procedures, Tasks, Functions and Verification:

Mixed type descriptions, Procedures and Tasks: Procedures (VHDL), Tasks (Verilog), Examples of Procedures and Tasks, Functions in VHDL & Verilog HDL.

Verification: Introduction to verification, simulation, static timing Analysis, Association languages and formal verification.

5. Individual time table

DAY/PERIOD	1	2	3	4	5	6	7
MON		D			C		
TUE		C				D	
WED			C		D		
THU	D		C				
FRI							
SAT	C				D		

6. Session Plan

Topic Name	No. of classes	Text books
UNIT I: SPLD, CPLD, FPGA		
Programmable Read Only Memories	1	T1
Programmable Logic Arrays	1	T1
Programmable Array Logic	1	T1
Masked Gate Array ASIC	1	T1
CPLD Architectures, Function Blocks	2	T1
I/O Blocks, Clock Drivers	1	T1
Interconnect CPLD Technology and Programmable Elements	1	T1
Embedded Devices	1	T1
FPGA Architectures, Configurable Logic Blocks	2	T1
Configurable I/o Blocks, Embedded Devices	1	T1
Programmable Interconnect, Clock Circuitry	2	T1
SRAM vs. Anti-fuse programming, FPGA Selection Criteria	2	T1
Total No. of Classes	16	
UNIT II: Universal Design Methodology for Programmable Devices		
Introduction to UDM and UDM-PD, writing a Specification	1	T1
Specification Review, Choosing Device and Tools	1	T1
Design, Verification, Final Review	1	T1
System Integration and Test	1	T1
Hardware Descriptive Languages, Structure of VHDL & Verilog module	1	T1, R1
Operator, Data types, Top-Down Design	2	T1, R1

Synchronous Design, Floating Nodes	1	T1, R1
Bus Contention, One-Hot state Encoding	1	T1, R1
Total No. of Classes	09	
UNIT III: Data flow Description and Behavioral Descriptions		
Introduction to styles types of hardware description	1	T2, R1
Behavioral, Structural, Dataflow and Mixed type and language descriptions	2	T2, R1
Structure of the dataflow description, Signal Declaration and Assignment Statements	2	T2, R1
Concurrent Signal assignments, Constant declaration and assignments	1	T2, R1
Assigning a delay time to the signal, Data type-Vectors	1	T2, R1
Structure of the HDL Behavioral description, The VHDL/ Verilog HDL variable	1	T2, R1
Assignment statement, sequential statement – IF	2	T2, R1
Signal and variable assignment, CASE & LOOP statements	2	T2, R1
Total No. of Classes	12	
UNIT IV: Structural and Switch level Descriptions		
Organization of the structural description, binding, state machines	1	T2, R1
Generate (HDL), Generic (VHDL), and parameter (Verilog)	2	T2, R1
Useful definitions, Single NMOS & PMOS switches	1	T2, R1
Verilog & VHDL description of NMOS & PMOS Switches	1	T2, R1
Serial and parallel combinations of switches	1	T2, R1
Switch level Description of –primitive gates,	1	T2, R1
Simple combinational logics	2	T2, R1
Simple sequential circuits, Bidirectional switches	2	T2, R1

Total No. of Classes	11	
UNIT V: Procedures, Tasks, Functions and Verification		
PProcedures (VHDL), Tasks (Verilog)	2	T2, R1
Examples of Procedures and Tasks	1	T2, R1
Functions in VHDL & Verilog HDL	2	T2, R1
Introduction to verification, simulation	1	T2, R1
Static timing Analysis, Association languages and formal verification	2	T2, R1
Total No. of Classes	08	
Total No. of Classes	56	

7. Session Execution Log

S.No	Topic	Execution Date
1	**UNIT I:** Programmable Read Only Memories	19/12/2022
2	Programmable Logic Arrays	20/12/2022
3	Programmable Array Logic, Masked Gate Array ASIC	21/12/2022
4	CPLD Architectures, Function Blocks	24/12/2022
5	I/O Blocks, Clock Drivers	26/12/2022
6	Interconnect CPLD Technology and Programmable Elements, Embedded Devices	27/12/2022
7	FPGA Architectures, Configurable Logic Blocks	28/12/2022
8	Configurable I/o Blocks, Embedded Devices	29/12/2022
9	Programmable Interconnect, Clock Circuitry	31/12/2022

10	SRAM vs. Anti-fuse programming, FPGA Selection Criteria	02/01/2023
11	**UNIT II:** Introduction to UDM and UDM-PD, writing a Specification	03/01/2023
12	Specification Review, Choosing Device and Tools	04/01/2023
13	Design, Verification, Final Review, System Integration and Test	05/01/2023
14	Hardware Descriptive Languages,	10/01/2023
15	Structure of VHDL & Verilog module	11/01/2023
16	Operators	12/01/2023
17	Data types	18/01/2023
18	Top-Down Design	19/01/2023
19	Synchronous Design, Floating Nodes	23/01/2023
21	Bus Contention, One-Hot state Encoding	24/01/2023
22	**UNIT III** :Introduction to styles types of hardware description	25/01/2023
23	Behavioral, Structural	28/01/2023
24	Dataflow and Mixed type and language descriptions	28/01/2023
25	Structure of the dataflow description	30/01/2023
26	Signal Declaration	31/01/2023
27	Assignment Statements	02/02/2023
28	Concurrent Signal assignments	06/02/2023
29	Constant declaration and assignments	08/02/2023
30	Assigning a delay time to the signal	11/02/2023
31	Data type-Vectors	14/02/2023

32	Structure of the HDL Behavioral description, The VHDL/ Verilog HDL variable	28/02/2023
33	Assignment statement	02/03/2023
34	Sequential statement – IF	04/03/2023
35	Signal and variable assignment	07/03/2023
36	CASE statements	09/03/2023
37	LOOP statements	13/03/2023
38	**UNIT IV** :Organization of the structural description	14/03/2023
39	Binding	15/03/2023
40	State machines	16/03/2023
41	Generate (HDL)	18/03/2023
42	Generic (VHDL)	20/03/2023
43	Parameter (Verilog)	21/03/2023
44	Useful definitions	23/03/2023
45	Single NMOS & PMOS switches	25/03/2023
46	Verilog & VHDL description of NMOS & PMOS Switches	28/03/2023
47	Serial and parallel combinations of Switches	29/03/2023
48	Switch level Description of –primitive gates	01/04/2023
49	Simple combinational logics	03/04/2023
50	Simple sequential circuits, Bidirectional switches	04/04/2023
51	**UNIT V:** Procedures (VHDL)	05/04/2023
52	asks (Verilog)	06/04/2023
53	Examples of Procedures and Tasks	08/04/2023

54	Functions in VHDL & Verilog HDL	10/04/2023
55	Introduction to verification, simulation	11/04/2023
56	Static timing Analysis, Association languages and formal verification	13/04/2023

8. Assignment Questions and Innovative assignments

Assignment Questions:

III.B.TECH- II-SEM FPGAP ASSAIGNMENT-I

SET-I

1. Explain the architectures of PLA and PAL ? [BL 1][CO 1]
2. Draw the CPLD I/O Block and explain in detail. [BL 1][CO 1]
3. Draw the UDM-PD flow chart and explain in detail. [BL 2][CO 2]
4. Explain the VHDL Operators. [BL 2][CO 2]
5. Write VHDL and Verilog code for Full Adder using two Half Adders. [BL 5][CO 5]

SET-II

1. Illustrate CPLD architecture and Function Block. [BL 2][CO 2]
2. Draw the FPGA I/O Block and explain in detail. [BL 2][CO 2]
3. What are the issues involved in Synchronous design? Explain in detail. [BL 2][CO 2]
4. Explain the Verilog Operators. [BL 2][CO 2]
5. Write VHDL and Verilog code for Full Adder. [BL 5][CO 5]

SET-III

1. Illustrate CPLD architecture and Function Block. [BL 2][CO 2]
2. Explain SRAM and Antifuse programming technologies. [BL 2][CO 2]
3. Explain in detail Top Down design methodology. [BL 5][CO 5]
4. Explain different styles types of design description in HDL. [BL 2][CO 2]
5. Write VHDL and Verilog code for Full Adder. [BL 2][CO 2]

III.B.TECH- II-SEM FPGAP ASSAIGNMENT-II

SET-I

1.Explain the structure of behavioral description? Give one example? [BL 1][CO 3]
2.Write VHDL and Verilog description of logical shifting of a register using loop statement? [BL 4][CO 3]
3.Explain the organization of structural description with an example? [BL 2][CO 4]
4. Explain switch level description of primitive gates? Give an example? [BL 2][CO 4]
5. What is simulation? What are the types of simulation? [BL 2][CO 5]

SET-II

1. Write VHDL and Verilog description for 2*1 multiplexer? [BL 4][CO 3]
2. Write VHDL and Verilog description of 4 bit counter with synchronous clear? [BL 4][CO 3]
3. Write structural description of 3 bit two stage carry save adder? [BL 4][CO 4]
4. Explain switch level description of combinational circuits? Give an example? [BL 2][CO 4]
5. Explain VHDL and verilog description of full adder using procedure and task? [BL 2][CO 3]

SET-III

1. Write VHDL and Verilog description for 3 bit binary counter using case statement? [BL 4][CO 3]
2. Write Verilog description of a 4 bit priority Encoder using casex? [BL 4][CO 3]
3. Explain structural description of a 3 bit synchronous counter? [BL 2][CO 4]
4. Explain switch level description of SR latch? [BL 2][CO 4]
5. Why mixed type description is used in HDL code? Explain with an Example? [BL 2][CO 5]

Innovative Assignment:

1. Design a PROM for the following expressions. (CO1)
   F0=A'B'C+AB'C'+AB'C
   F1=A'B'C+A'BC'+ABC
   F2=A'B'C'+A'B'C+AB'C'
   F3=A'BC+AB'C'+ABC'
2. Design a programmable logic array mapping algorithm for CPLD's. (CO2)
3. Explain how delay times of arithmetic circuits are solved using FPGA/ASIC co-design? (CO3)
4. Design a video driver system using top –down approach. (CO4)
5. Illustrate one hot encoding FSM in SRAM based FPGA's. (CO5)

13. Unit wise Course Material

14. Material collected from Internet/Websites

15. Power Point Presentations

17. Previous Question Papers

18. References (Text books/websites/Journals)

TEXT BOOKS:

1. Designing with FPGAS & CPLDS- Bob Zeidman, CMP Books, First Printed in India2011
2. HDL Programming Fundamental-VHDL & Verilog, Botros, Cengage Learning, ThirdIndian Reprint 2012

REFERENCE BOOKS:

1. Verilog HDL: A guide to Digital Design and Synthesis, Samir Palnitkar, Pearson

WEBSITES:

1. https://youtu.be/gCAYY0fHPq4
2. https://youtu.be/dQDIWFxmP2E
3. https://youtu.be/_IgaKFKg3H8
4. https://youtu.be/wANFPIPIC9Q
5. https://fpgatutorial.com
6. https://www.electronics-tutorial.net/programmable-logic-devices/complex-programmable-logic-device/
7. https://www.asic-world.com/verilog/veritut.html
8. https://nandland.com/introduction-to-vhdl-for-beginners-with-code-examples/

JOURNALS:

1. Routing Architecture and Applications of FPGA: A survey

https://iopscience.iop.org/article/10.1088/1742-6596/1717/1/012025/pdf

2. The Detection of Malicious Modifications in the FPGA
https://dl.acm.org/doi/abs/10.1007/s10836-022-06004-z

3. A Real-Time Image Processing with a Compact FPGA-Based Architecture
https://www.design-reuse.com/articles/10943/a-real-time-image-processing-with-a-compact-fpga-based-architecture.html

4. High Performance Programmable FPGA Overlay for Digital Signal Processing
https://link.springer.com/chapter/10.1007/978-3-642-19475-7_39

5. Efficient FPGA Implementation of an RFIR Filter Using the APC–OMS Technique with WTM for High-Throughput Signal Processing
https://www.mdpi.com/2079-9292/11/19/3118

9. Sample Assignment Script

12. Sample Mid Answer Script