A

Course File Report

on

“ LOW POWER VLSI DESIGN”

Submitted by

Ms. P.RANI

Assistant Professor

In the department of

Electronics & Communication Engineering

CMR ENGINEERING COLLEGE

(Affiliated to J.N.T.U, HYDERABAD)

KANDLAKOYA (V), MEDCHAL ROAD HYDERABAD - 501 401

(2022-2023)

Department of Electronics & Communication Engineering

COURSE FILE

Sub: LOW POWER VLSI DESIGN **AY: 2022-2023**

Year: IV Year II Semester

CONTENTS

1. **DEPARTMENT VISION & MISSION**

VISION OF THE DEPARTMENT

To promote excellence in technical education and scientific research in electronics and communication engineering for the benefit of society.

2. **MISSION OF THE DEPARTMENT**

M1: To impart excellent technical education with state of art facilities inculcating values and lifelong learning attitude.

M2: To develop core competence in our students imbibing professional ethics and team spirit.

M3: To encourage research benefiting society through higher learning.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO 1: Establish themselves as successful professionals in their career and higher education in the field of Electronics & Communication Engineering and allied domains through rigorous quality education.

PEO 2: Develop Professionalism, Ethical values, Excellent Leadership qualities, Communication Skills and teamwork in their Professional front and adapt to current trends by engaging in lifelong learning

PEO 3: Apply the acquired knowledge & skills to develop novel technology and products for solving real life problems those are economically feasible and socially relevant

PEO 4: To prepare the graduates for developing administrative acumen, to adapt diversified and multidisciplinary platforms to compete globally

PROGRAM SPECIFIC OUTCOMES (PSOs)

PSO1: Ability to apply concepts of Electronics & Communication Engineering to associated research areas of electronics, communication, signal processing, VLSI, embedded systems, IoT and allied technologies.

PSO2: Ability to design, analyze and simulate a variety of Electronics & Communication functional elements using hardware and software tools along with analytic skills.

Program Outcomes (POs) :

PO1:Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2:Problem analysis: Identify, formulate, review research literature and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3:Design/Development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4:Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5:Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6:The Engineer and Society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7:Environment and Sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8:Ethics: Apply ethical principles and commit to professional ethics

and responsibilities and norms of the engineering practice.

PO9:Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10:Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11:Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12:Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

3. COURSE OUTCOMES and MAPPING WITH POS

Course Outcomes: Having gone through this course covering different aspects of microwave theory and techniques, the students would be able to		**Blooms Level's**
CO1	Understand the need fo Low-Power circuit diagram..	BL2
CO2	Demonstrate the Low-Power design and Switched Capacitance Minimization Approaches.	BL3
CO3	Analyze and design Low-Voltage Low-Power combinational circuits	BL4
CO4	Discuss the design of Low-Voltage Low-Power Memories	BL2
	Designing of Low-Voltage Low-Power Multiplier.	BL6

Course Outcome (CO)-Program Outcome (PO) Matrix:

Course Outcomes (CO)	**PO1**	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	2	2	2	2		-	-	-	-	-	-	-
CO2	3	-	3	-	-	-	-	-	-	-	-	-
CO3	2	2	3	-	3	-	-	-	2	-	-	-
CO4	2	3	3	-	-	-	-	-	2	-	-	-
CO5	2	3	2									

Course Outcome (CO)-Program Specific Outcome (PSO) Matrix:

Course Outcomes (CO's)	PSO1	PSO2
CO1	2	3
CO2	3	-
CO3	3	2
CO4	3	3
CO5	2	2
AVG	3	3

4. SYLLABUS COPY

LOW POWER VLSI DESIGN

B.Tech. IV Year II Sem **L T P C**

Course Code: EC823PE **3 0 0 3**

Course Objectives:

- Known the low power low voltage VLSI design
- Understand the impact of power on system performances.
- Known about different Design approaches.
- Identify suitable techniques to reduce power dissipation in combinational and sequentialcircuits.

Course Outcomes: Upon completing this course, the student will be able to

- Understand the need of Low power circuit design.
- Attain the knowledge of architectural approaches.
- Analyze and design Low-Voltage Low-Power combinational circuits.
- Known the design of Low-Voltage Low-Power Memories

UNIT – I

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT – II

Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures,and Mask level Measures

UNIT – III

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures Ripple Carry Adders, Carry Look- Ahead Adders, Carry Select Adders, Carry Save

Adders, Low- Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low- Voltage Low-Power Logic Styles.

UNIT - IV

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier, Introduction to Wallace TreeMultiplier.

.

UNIT – V

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici,TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH ProfessionalEngineering.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRCPress, 2011
2. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons,2000.
3. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
4. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, Anatha Chandrakasan,Springer, 2005.

5. INDIVIDUAL TIME TABLE

DAY/ TIME	9.10 - 10.10	10.10-11.00	11.00 – 11.50	11.50 to 12.40	12.40 to 1.20	1.20 to 2.20	2.20 to 3.10	3.10 to 4.00
MON	LPVLSID-A			LPVLSID-A	LUNCH BREAK	ECALAB -A		
TUE		ECALAB -C					LPVLSID-A	
WED		ECALAB -A				LPVLSID-A		
THU	LPVLSID-A	LPVLSID-A				ECALAB -C		
FRI		ECALAB-D					LPVLSID-A	
SAT			LPVLSID-A			ECALAB-D		

6. LESSION PLAN

UNIT NO.	NAME OF THE UNIT	NO.OF LECTURES REQUIRED
UNIT I	Fundamentals	12
UNIT II	Low-Power Design Approaches	10
UNIT III	Low-Voltage Low-Power Adders	08
UNIT IV	Low-Voltage Low-Power Multipliers	07
UNIT V	Low-Voltage Low-Power Memories	10

7. DETAILED LESSON PLAN

S. No	Topic to be Covered	Suggested Books (Eg. T1, T2,R1)	CO'S	No. of Lectures Required
	UNIT-I			
1	Introduction to **Fundamentals**	**T1,R1**	CO1	1
2	Need for Low Power Circuit Design	T1		1
3	Sources of Power Dissipation Switching PowerDissipation	T1,R2,R3		2
4	Short Circuit Power Dissipation Leakage Power Dissipation, Glitching Power Dissipation	T1,R2		2
5	Short Channel Effects Drain Induced Barrier Lowering and Punch Through	T1,R1		3
6	Drain Induced Barrier Lowering and Punch Through	T2		1
7	Surface Scattering, Velocity Saturation Impact Ionization, Hot Electron Effect	T1,R2		2
	TOTAL NO.OF CLASSES :12			
	UNIT-II			
8	Low-PowerDesign Approaches Low-Power Design through Voltage Scaling	T1,R2	CO2	2
9	VTCMOS circuits MTCMOS circuits	T2,R2		2
10	Architectural Level Approach Pipelining and Parallel Processing Approaches	T2,R2,R3		2
11	Switched Capacitance Minimization Approaches System Level Measures	T1,R2		2
12	Circuit Level Measures Mask level Measures.	T1,R2,R3		2
		TOTAL NO.OF CLASSES :10		
		UNIT-III		
13	**Low-Voltage Low-Power Adders:** Introduction Standard Adder Cells	T1,R2,R3	CO3	1

14	CMOS Adder's Architectures Ripple Carry Adders Carry Look- Ahead Adders	T1,R3		2
15	Carry Select Adders Carry Save Adders	T1,R2		1
16	Low- Voltage Low-Power Design Techniques Trends of Technology	T1,R3		2
17	Power Supply Voltage Low- Voltage Low-Power Logic Styles	T1,R3		2
	TOTAL NO.OF CLASSES :08			
	UNIT-IV			
18	Low-Voltage Low-Power Multipliers	T2,R2,R3	CO4	2
19	Introduction, Overview of Multiplication Types of Multiplier Architectures	T2,R2,R3		2
20	Braun Multiplier Baugh Wooley Multiplier.	T2,R2,R3		2
21	Booth Multiplie Introduction to Wallace Tree Multiplier	T2,R2,		1
TOTAL NO.OF CLASSES :7				
UNIT-V				
22	Low-Voltage Low-Power Memories	T2,R1,R3	CO5	2
23	Basics of ROM, Low-Power ROM Technology	T2,R1,R3		2
24	Future Trend and Development of ROMs Basics of SRAM, Memory Cell	T2,R2		2
25	Precharge and Equalization Circuit Low-Power SRAM Technologies	T2,R3		2
26	Basics of DRAM, Self-Refresh Circuit Future Trend and Development of DRAM.	T2,R3		2
TOTAL NO.OF CLASSES :10				

8. SESSION EXECUTION LOG:

S .no	Syllabus	No. Classes	Remarks
1	I-UNIT	12	COMPLETED
2	II-UNIT	10	COMPLETED
3	III-UNIT	08	COMPLETED
4	IV-UNIT	07	COMPLETED
5	V-UNIT	10	COMPLETED

9. ASSIGNMENT QUESTIONS:

CMR ENGINEERING COLLEGE

Kandlakoya (v), Medchal Road, Hyderabad -501401

IV.B.TECH II-SEM I- MID ASSIGNMENT QUESTIONS Subject: LPVLSID

SET - 1

What are the different approaches to minimize the capacitance? Explain them in detail?(C02)

2. What are different types of power dissipation in CMOS circuits and discuss any

Three methods in detail. (CO1)

3. Explain the basic concepts of supply voltage scaling(CO2)

4. Discuss the need of low power VLSI design (CO1))

SET - 2

1a) What are the various limitations of Low-voltage, Low-power design (CO1)

2) Briefly discuss about pipelining and parallel processing approaches with suitable examples? (CO2)

3)Draw the schematic of an MTCMOS circuit and explain its working? (CO2)

4) What are the different approaches to minimize the capacitance? Explain them in detail? (CO2)

SET - 3

1)Explain the basic concepts of supply voltage scaling. (CO2)

2) A)Briefly discuss about pipelining and parallel processing approaches with suitable

examples.(CO3)

B)What are the three sources of power dissipation? Explain.

3)Write the advantages and disadvantages of MTCMOS circuits.(CO2)

4) Explain Low-Power Design through Voltage Scaling – VTCMOS circuits(CO1)

CMR ENGINEERING COLLEGE
Kandlakoya (V), Medchal Road, Hyderabad – 501401

IVB.TECH. II SEM MID-2 ASSIGNMENT QUESTIONS SUBJECT: LPVLSID

Set 1

1. What are the different Techniques of Low Voltage Low Power Techniques? And explain (C02)
2. Explain details about Types of Multitier Architectures? (CO1)
3. Explain the Low Power ROM Technology ?(CO2)
4. Write short notes on(CO3)

a) Ripple Carry Adder(RCA)

b) Carry look –ahead Adder (CLA)

Set2

1. Basics of ROM, Low-Power ROM Technology(CO3)
2. Briefly explain Low- Voltage Low-Power Logic Styles(CO4)
3. Write short notes on Baugh- Wooley Multiplier(CO2)
4. Circuit Level Measures,and Mask level Measures.(CO3)

Set3

1. Define Low-Power ROM Technology(CO4)
2. Basics of SRAM, Memory Cell(CO4)
3. Explain Future Trend and Development of DRAM(CO3)
4. Explain Booth Multiplier, Introduction to Wallace TreeMultiplier.(CO2)

10. SAMPLE ASSIGNMENT SCRIPT:

(Attached separately)

11. UNIT WISE COURSE MATERIAL:

LPVLSID notes.rar

12. MID EXAM QUESTION PAPERS

CMR ENGINEERING COLLEGE
Kandlakoya (v), Medchal Road, Hyderabad -501401

IV.B.TECH II-SEM (R18)-I MID EXAMINATIONS, NOV-2023 ***Date*: 9.05.2023 FN**
Subject: LPVLSID **Branch: CSE** **Time: 1hr** **Marks: 2X5=10 M**

Answer any TWO Questions:

1.What are the different approaches to minimize the capacitance? Explain them in detail?(C02)
2. What are different types of power dissipation in CMOS circuits and discuss any Three methods in detail. (CO1)
3. Explain the basic concepts of supply voltage scaling(CO2)
4. Discuss the need of low power VLSI design (CO1)

Scheme of Evaluation

S.NO	THEORY	MARKS	TOTAL
1	different approaches to minimize the capacitance	2	5
	Detailed explanation	3	
2	different types of power dissipation in CMOS circuit	1	5
	Three methods explanation and diagram	4	
3	Basic concept of supply voltage scaling	2	5
	explanation the basic concept	3	
4	low power VLSI design explanation	3	5
	low power VLSI design Diagram	2	

CMR ENGINEERING COLLEGE
Kandlakoya (v), Medchal Road, Hyderabad -501401

IV.B.TECH II-SEM (R18)-II MID EXAMINATIONS, FEB-2023 ***Date*: 19.6.2023 FN**
Subject: LPVLSID **Branch: CSE** **Time: 1hr** **Marks: 2X5=10 M**

Answer any TWO Questions:

1. What are the different Techniques of Low Voltage Low Power Techniques? And explain (C02)
2. Explain details about Types of Multitier Architectures? (CO1)
3. Explain the Low Power ROM Technology ?(CO2)
4. Write short notes on(CO3)

a) Ripple Carry Adder(RCA) b) Carry look –ahead Adder (CLA)

Scheme of Evaluation

S.NO	THEORY	MARKS	TOTAL
1	Low Voltage Low Power Techniques explanation	4	5
	Formulas	1	
2	Multitier Architectures definition and diagram	2	5
	Explanation of various types of Multitier Architectures	3	
3	Low Power ROM Technology Explanation	2	5
	Low Power ROM Technology Diagram	3	
4	Ripple Carry Adder(RCA) Importance	3	5
	Carry look –ahead Adder	2	

13. SAMPLE MID ANSWERS SCRIPTS

(Attached Separately)

14. MATERIAL COLLECTED FROM INTERNET OR WEBSITES:

1.https://www.youtube.com/watch?v=ORtlxpW_LMU

2. https://www.youtube.com/watch?v=N65OEIlX_Wc

3.https://www.youtube.com/watch?v=ruClwamT-R0&list=PLTEh-62_zAfHmJE-pcjgREKiKyPSgjkxj

4. https://www.youtube.com/watch?v=TFOO1JAll2Y

5.https://www.youtube.com/watch?v=_A7fUR2Itsc

15. POWER POINT PRESENTATIONS (PPTS):

lpvlsid ppt.rar

16. Innovation teaching methods (if any):

1.LIST OF STUDENT SEMINARS:

1. Introduction to VLSI Technology
2. Explain about Low-Voltage Low-Power Switched Capacitance
3. Explain about Low-Voltage Low-Power Adders
4. Explain about Low-Voltage Low-Power Multipliers
5. Explain about Low-Voltage Low-Power Memories

17. UNIVERSITY QUESTION PAPERS/ QUESTION BANK:

LPVLSID PQ.rar

18. REFERENCES (TEXTBOOKS/WEBSITES/JOURNALS)

TEXT BOOKS:

3. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici,TMH, 2011.
4. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH ProfessionalEngineering.

WEBSITES

1.http://nptel.ac.in
2.https://www.youtube.com/watch?v=nmLw3ONx8L8
3.https://www.electronics-tutorials.ws/blog/voltage-multiplier-circuit.html

INTERNATIONAL

1 Mrs.Avirup Dasgupta, Ph. D. Assistant Professor (Semiconductors)

ECE Department, IIT Roorkee, Uttarakhand, India. PIN: 247667
Phone: (+91-1332)28-4967)-Office
Email: avirup@ece.iitr.ac.in

2 Arnab Datta,Ph.D. Associate Professor (VLSI),

ECE Department, IIT Roorkee, Uttarakhand, India. PIN: 247667

PHONE: (+91-1332-285464)-Office

Email: arnab.datta@ece.iitr.ac.in

NATIONAL

1.Dr.ROBERT FOX(Analog Integrated Circuit Design), associate professor AND ECE ASSOCIATE CHAIR at the University of Florida. Email: fox@tec.ufl.edu

Phone: 352-392-2543

Mailing Address: P.O. Box 116130, Gainesville, FL 32611-6130

2.Dr.Abeer Alwan , ECE Department Vice Chair of Undergraduate Affairs was a member of the faculty of the UCLA Samueli School of Engineering

Email: alwan@ee.ucla.edu
Phone: (310) 206-2231

REGIONAL

1. 1 Dr. Mohammad Farukh Hashmi, Assistant Professor, ECE Department, NIT, Warangal

   E-Mail: mdfarukh@nitw.ac.in
   Phone No: 9666740604
2. Dr. T. Kishore Kumar, Professor , ECE Department, NIT, Warangal
   E-Mail: kishoret@nitw.ac.in,kishorefr@gmail.com
   Phone No: 8332969353, 9440973318

JOURNALS

1. https://ieeexplore.ieee.org/document/7164842
2. https://ieeexplore.ieee.org/document/8392017
3. https://ieeexplore.ieee.org/document/6524492
4. https://ieeexplore.ieee.org/document/7543188
5. https://ieeexplore.ieee.org/document/996775