CMR ENGINEERING COLLEGE

UGC AUTONOMOUS

(Approved by AICTE - New Delhi. Affiliated to JNTUH and Accredited by NAAC & NBA)

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

COURSE INSTRUCTOR NAME: Dr. Monika Arya **ACADEMIC YEAR**:2024-25

SUBJECT NAME: Computer Organization and Architecture **SECTION:** E & F

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SEM START DATE AND END DATE: 18-9-23 **T0** 20-01-24

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1. DEPARTMENT VISION & MISSION

VISION:

To produce globally competent and industry-ready graduates in Computer Science & Engineering by imparting quality education with the know-how of cutting-edge technology and holistic personality.

MISSION:

1. To offer high-quality education in Computer Science & Engineering in order to build core competence for the graduates by laying a solid foundation in Applied Mathematics and program frameworkwith a focus on concept building.
2. The department promotes excellence in teaching, research, and collaborative activities to prepare graduates for a professional career or higher studies.
3. Creating an intellectual environment for developing logical skills and problem-solving strategies, thus developing, an able and proficient computer engineer to compete in the current global scenario.

2. LIST OF PEOs, POs AND PSOs

2.1 Program Educational Objectives (PEO):

PEO 1: Excel in professional career and higher education by acquiring knowledge of mathematical computing and engineering principles.
PEO 2: To provide an intellectual environment for analyzing and designing computing systems for technical needs.
PEO 3: Exhibit professionalism to adapt current trends using lifelong learning with legal and ethical responsibilities.
PEO 4: To produce responsible graduates with effective communication skills and multidisciplinary practices to serve society and preserve the environment.

2.2. Program Outcomes (POs):

Engineering Graduates will be able to satisfy these NBA graduate attributes:

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

2. **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

7. **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

8. **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

9. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

10. **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one’s own work, as a member and

leader in a team, to manage projects and in multidisciplinary environments.

11. **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

2.3 Program Specific Outcomes (PSOs):

PSO1: Professional Skills and Foundations of Software development: Ability to analyze, design and develop applications by adopting the dynamic nature of Software developments.
PSO2: Applications of Computing and Research Ability: Ability to use knowledge in cutting edge technologies in identifying research gaps and to render solutions with innovative ideas.

3. COURSE OUTCOMES

S. No	Course Out Come

CO1	**Define** the basic components of a digital computer. Understand the basics of micro-operations and the architecture of modern computers.
CO2	**Describe** arithmetic logic and shift micro-operations in symbolic form at a register transfer level. Develop the assembly language programming and demonstrate the addressing modes used in instructions.
CO3	**Apply** algorithm for arithmetic operations and implementations of ALU design.
CO4	**Understand** the concepts of memory hierarchy and organization.
CO5	**Recognize** the concepts of parallel processing, pipelining, and inter-processor communication. Design 3 and 4-stage pipeline processor.

REVISED Bloom's Taxonomy Action Verbs

Definitions	I. Remembering	II. Understanding	III. Applying	IV. Analyzing	V. Evaluating	VI. Creating
Bloom's Definition	Exhibit memory of previously learned material by recalling facts, terms, basic concepts, and answers.	Demonstrate understanding of facts and ideas by organizing, comparing, translating, interpreting, giving descriptions, and stating main ideas.	Solve problems to new situations by applying acquired knowledge, facts, techniques and rules in a different way.	Examine and break information into parts by identifying motives or causes. Make inferences and find evidence to support generalizations.	Present and defend opinions by making judgments about information, validity of ideas, or quality of work based on a set of criteria.	Compile information together in a different way by combining elements in a new pattern or proposing alternative solutions.
Verbs	• Choose • Define • Find • How • Label • List • Match • Name • Omit • Recall • Relate • Select • Show • Spell • Tell • What • When • Where • Which • Who • Why	• Classify • Compare • Contrast • Demonstrate • Explain • Extend • Illustrate • Infer • Interpret • Outline • Relate • Rephrase • Show • Summarize • Translate	• Apply • Build • Choose • Construct • Develop • Experiment with • Identify • Interview • Make use of • Model • Organize • Plan • Select • Solve • Utilize	• Analyze • Assume • Categorize • Classify • Compare • Conclusion • Contrast • Discover • Dissect • Distinguish • Divide • Examine • Function • Inference • Inspect • List • Motive • Relationships • Simplify • Survey • Take part in • Test for • Theme	• Agree • Appraise • Assess • Award • Choose • Compare • Conclude • Criteria • Criticize • Decide • Deduct • Defend • Determine • Disprove • Estimate • Evaluate • Explain • Importance • Influence • Interpret • Judge • Justify • Mark • Measure • Opinion • Perceive • Prioritize • Prove • Rate • Recommend • Rule on • Select • Support • Value	• Adapt • Build • Change • Choose • Combine • Compile • Compose • Construct • Create • Delete • Design • Develop • Discuss • Elaborate • Estimate • Formulate • Happen • Imagine • Improve • Invent • Make up • Maximize • Minimize • Modify • Original • Originate • Plan • Predict • Propose • Solution • Solve • Suppose • Test • Theory

Anderson, L. W., & Krathwohl, D. R. (2001). A taxonomy for learning, teaching, and assessing, Abridged Edition. Boston, MA: Allyn and Bacon.

Action Words for Bloom's Taxonomy					
Knowledge	**Understand**	**Apply**	**Analyze**	**Evaluate**	**Create**
define	explain	solve	analyze	reframe	design
identify	describe	apply	compare	criticize	compose
describe	interpret	illustrate	classify	evaluate	create
label	paraphrase	modify	contrast	order	plan
list	summarize	use	distinguish	appraise	combine
name	classify	calculate	infer	judge	formulate
state	compare	change	separate	support	invent
match	differentiate	choose	explain	compare	hypothesize
recognize	discuss	demonstrate	select	decide	substitute
select	distinguish	discover	categorize	discriminate	write
examine	extend	experiment	connect	recommend	compile
locate	predict	relate	differentiate	summarize	construct
memorize	associate	show	discriminate	assess	develop
quote	contrast	sketch	divide	choose	generalize
recall	convert	complete	order	convince	integrate
reproduce	demonstrate	construct	point out	defend	modify
tabulate	estimate	dramatize	prioritize	estimate	organize
tell	express	interpret	subdivide	find errors	prepare
copy	identify	manipulate	survey	grade	produce
discover	indicate	paint	advertise	measure	rearrange
duplicate	infer	prepare	appraise	predict	rewrite
enumerate	relate	produce	break down	rank	role-play
listen	restate	report	calculate	score	adapt
observe	select	teach	conclude	select	anticipate
omit	translate	act	correlate	test	arrange
read	ask	administer	criticize	argue	assemble
recite	cite	articulate	deduce	conclude	choose
record	discover	chart	devise	consider	collaborate
repeat	generalize	collect	diagram	critique	collect
retell	give examples	compute	dissect	debate	devise
visualize	group	determine	estimate	distinguish	express
	illustrate	develop	evaluate	editorialize	facilitate
	judge	employ	experiment	justify	imagine
	observe	establish	focus	persuade	infer
	order	examine	illustrate	rate	intervene
	report	explain	organize	weigh	justify
	represent	interview	outline		make
	research	judge	plan		manage
	review	list	question		negotiate
	rewrite	operate	test		originate
	show	practice			propose
	trace	predict			reorganize
	transform	record			report
		schedule			revise
		simulate			schematize
		transfer			simulate
		write			solve
					speculate
					structure
					support
					test
					validate

4. SYLLABUS COPY

UNIT – I

Digital Computers: Introduction, Block diagram of Digital Computer, Definition of Computer Organization, Computer Design and Computer Architecture.

Register Transfer Language and Micro operations: Register Transfer language, Register Transfer, Bus and memory transfers, Arithmetic Micro operations, logic micro operations, shift micro operations, Arithmetic logic shift unit.

Basic Computer Organization and Design: Instruction codes, Computer Registers Computer Instructions, Timing and Control, Instruction cycle, Memory Reference Instructions, Input – Output and Interrupt.

UNIT – II

Micro programmed Control: Control memory, Address sequencing, micro program example, design of control unit.
Central Processing Unit: General Register Organization, Instruction Formats, Addressing modes, Data Transfer and Manipulation, Program Control.

UNIT – III

Data Representation: Data types, Complements, Fixed Point Representation, Floating Point Representation.
Computer Arithmetic: Addition and subtraction, multiplication Algorithms, Division Algorithms, Floating – point Arithmetic operations. Decimal Arithmetic unit, Decimal Arithmetic operations.

UNIT – IV

Input-Output Organization: Input-Output Interface, Asynchronous data transfer, Modes of Transfer, Priority Interrupt Direct memory Access.
Memory Organization: Memory Hierarchy, Main Memory, Auxiliary memory, Associate Memory, Cache Memory.

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UNIT – V

Reduced Instruction Set Computer: CISC Characteristics, RISC Characteristics.
Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processor.
Multi Processors: Characteristics of Multiprocessors, Interconnection Structures, Interprocessor Arbitration, Interprocessor communication and synchronization, Cache Coherence.

TEXT BOOK:

1. **Computer System Architecture** – M. Moris Mano, Third Edition, Pearson/PHI.

REFERENCES:

1. **Computer Organization** – Car Hamacher, Zvonks Vranesic, Safea Zaky, Vth Edition, McGraw Hill.
2. **Computer Organization and Architecture** – William Stallings Sixth Edition, Pearson/PHI.
3. **Structured Computer Organization** – Andrew S. Tanenbaum, 4th Edition, PHI/Pearson.

5. INDIVIDUAL TIME TABLE (Dr. Monika Arya)

	I	II	III	IV		V	VI	VII
MON				COA-F				
TUE								
WED			COA-E			COA-F		
THU				COA-F			COA-E	
FRI						COA-E		COA-F
SAT			COA-F				COA-E	

LUNCH

6. SESSION PLAN/LESSON PLAN

s.no	Topic (JNTU syllabus)	Sub-topic	No. of lectures required	Suggested books	Teaching methods
UNIT 1					
1	**Digital Computer, Register Transfer Language and Micro operations, Basic Computer Organization And Design**	Introduction, Block diagram of Digital Computer	L1	T1	M1,M4
2		Definition of Computer Organization, Computer Design and Computer Architecture.	L2	T1	M1,M4
3		Instruction codes	L3	T1	M1,M4
4		Computer Registers	L4	T1	M1,M4
5		Computer instructions	L5	T1	M1,M4
6		Timing and Control	L6	T1	M1,M4
7		Instruction cycle	L7	T1	M1,M4
8		Memory Reference Instructions	L8	T1	M1,M4
9		Input – Output and Interrupt	L9	T1	M1,M4
10		Complete Computer Description	L10	T1	M1,M4
UNIT - II					
11	**Micro Programmed Control, CPU**	Control memory	L11	T2	M1,M4
12		Address sequencing	L12	T2	M1,M4
13		micro program example	L13	T2	M1,M4
14		General Register Organization	L14	T2	M1,M4
15		Instruction Formats	L15	T2	M1,M4
16		Addressing modes	L16	T2	M1,M4
17		Data Transfer and Manipulation	L17	T2	M1,M4
		Program Control.	L18	T2	M1,M4
18		design of control unit	L19	T2	M1,M4

UNIT - III					
19	**Data Representation, Computer Arithmetic**	Data Types	L20	T2	M1,M4
20		Complements	L21	T2	M1,M4
21		Fixed Point Representation	L22	T2	M1,M4
22		Floating Point Representation.	L23	T2	M1,M4
23		Addition And Subtraction	L24	T2	M1,M4
24		Multiplication Algorithms	L25	T2	M1,M4
25		Division Algorithms	L26	T2	M1,M4
26		Floating – Point Arithmetic Operations.	L27	T2	M1,M4
27		Decimal Arithmetic Unit	L28	T2	M1,M4
28		Decimal Arithmetic Operations.	L29	T2	M1,M4
UNIT-IV					
30	**I/O Organization, Memory Organization**	Peripheral Devices	L30	T1	M1,M4
31		Input-Output Interface	L31	T1	M1,M4
32		Asynchronous Data Transfer	L32	T1	M1,M4
33		Modes Of Transfer	L33	T1	M1,M4
34		Priority Interrupt	L34	T1	M1,M4
35		Direct Memory Access	L35	T1	M1,M4
36		Input –Output Processor (IOP)	L36	T1	M1,M4
37		Memory Hierarchy	L37	T1	M1,M4
38		Main Memory	L38	T1	M1,M4
39		Auxiliary Memory	L39	T1	M1,M4
40		Associate Memory	L40	T1	M1,M4
41		Cache Memory	L41	T1	M1,M4
UNIT-V					
42	**RISC, Pipeline and Vector Processing, Multiprocessor**	SISC AND RISC	L41	T1	M1,M4
43		Parallel Processing	L42	T1	M1,M4
44		Pipelining, Arithmetic Pipeline	L43	T1	M1,M4
45		Instruction Pipeline	L44	T1	M1,M4
46		RISC Pipeline	L45	T1	M1,M4
47		Vector Processing,	L46	T1	M1,M4
48		Characteristics Of Multiprocessors	L47	T1	M1,M4
49		Interconnection Structures	L48	T1	M1,M4
50		Inter-processor Arbitration	L49	T1	M1,M4
51		Array Processors	L50	T1	M1,M4
52		Inter Processor Communication, And	L51	T1	M1,M4

		Synchronization			

METHODS OF TEACHING:

M1: Lecture Method	**M4: Presentation /PPT**	**M7: Assignment**
M2: Demo Method	**M5: Lab/Practical**	**M8: Industry Visit**
M3: Guest Lecture	**M6: Tutorial**	**M9: Project Based**

NOTE:

1. Any Subject in a Semester is supposed to be completed in 55 to 65 periods.
2. Each Period is of 50 minutes.
3. Each unit duration &completion should be mentioned in the Remarks column.
4. ListofSuggestedbookscanbemarkedwithCodeslikeT1, T2, R1, R2etc.

7. SESSION EXECUTION LOG

S. no	Unit	Scheduled completed date	Completed date	Remarks
1	**I**	Sec F- 29/8/24 Sec E- 29/8/24	Sec F- 29/8/24 Sec E- 11/9/24	COMPLETED
2	**II**	Sec F- 20/9/24 Sec F- 20/9/24	Sec F- 23/9/24 Sec F- 21/9/24	COMPLETED
3	**III**	Sec F- 6/11/24 Sec F- 6/11/24	Sec F- 6/11/24 Sec F- 7/11/24	COMPLETED
4	**IV**	Sec F- 14/11/24 Sec F- 14/11/24	Sec F- 14/11/24 Sec F- 16/11/24	COMPLETED
5	**V**	Sec F- 25/11/24 Sec F- 25/11/24	Sec F- 25/11/24 Sec F- 26/11/24	COMPLETED

8. Lecture Notes (Hand Written)

9. Assignment Questions along with sample Assignments Scripts

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MID 1 ASSIGNMENT

ACADEMIC YEAR 2023-24

SUBJECT NAME: COMPUTER ORGANIZATION AND ARCHITECTURE

1 (a) **Explain** about Block Diagram of Digital computer.	**CO1**
(b) **Difference** between Computer Organization &Architecture.	**CO1**
2 (a) **Explain** about Micro Operations.	**CO1**
(b) **Define** Micro operations and explain various types of micro-operations with example.	**CO1**
3 (a) Draw arithmetic logic shift unit and **explain**.	**CO1**
(b) **Discuss** computer registers and computer instructions.	**CO1**
4 **Explain** about Instruction format and Instruction cycle.	**CO1**
5 (a) **Explain** about addressing modes	**CO2**
(b) **Explain** about Address sequencing	**CO2**

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MID II ASSIGNMENT

ACADEMIC YEAR 2023-24

SUBJECT NAME: COMPUTER ORGANIZATION AND ARCHITECTURE

1)Explain Multiplication Algorithm with Example.	**CO3**
2) Explain about Input-Output Interface with neat diagram?	**CO4**
3) Write about Asynchronous Data Transfer with methods?	**CO4**
4) Explain about Memory Hierarchy with neat diagram?	**CO4**
5) a) Distinguish CISC and RISC characteristics?	**CO5**
b) Explain types of Pipeline and Vector Processing?	**CO5**

10. Mid exam Question Papers along with sample Answers Scripts

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Kandlakoya (V), Medchal (M), Medchal - Malkajgiri (D)-501401

A.Y 2023-24
MID-I QUESTION PAPER
COMPUTER ORGANISATION AND ARCHITECTURE

Date: **Time: 10:00AM to 12:00PM**

Subject: C O A **Branch: CSE/IT/AIML**

Note: Question paper contains two parts, Part-A and Part- B.

Part-A is compulsory which carries 10 marks. Answer all questions in part-A.

Part-B Answer anyone full question from each unit. Each question carries5 marks.

PART-A **5x 2M =10 M**

		BTL	CO
1.	Compare Computer organization and Computer Architecture	**2**	**1**
2.	Define Register and list out the registers	**2**	**1**
3.	Explain about data transfer and data manipulation instructions	**1**	**2**
4.	Explain about microprogram examples?	**1**	**2**
5.	Explain complements with examples	**3**	**3**

PART-B **4 x 5 M = 20 M**

		BTL	CO
6.	Explain about timing and control with flow chart?	**3**	**1**
7.	Define BUS and explain about common bus system using decoders	**3**	**1**
8.	Explain about instruction cycle with flow chart?	**3**	**1**
9.	Discuss different types of addressing modes with examples?	**4**	**2**
10.	Explain about Design of control unit with neat diagram?	**3**	**2**
11. a)	Explain about datatypes	**2**	**3**

b) what is meant by fixed-point representation with examples **3** **3**

11. SCHEME OF EVALUATION

PART-A

SNO	THEORY	MARKS	TOTAL
1	Compare Computer organization and Computer Architecture	**2**	**2**
2	Define Register and list out the registers	**2**	**2**
3	Explain about data transfer and data manipulation instructions	**2**	**2**
4	Explain about microprogram examples?	**2**	**2**
5	Explain complements with examples	**2**	**2**

PART-B

SNO	THEORY	MARKS	TOTAL
6	Explain about timing and control with flow chart?	**5**	**5**
7	Define BUS and explain about common bus system using decoders	**5**	**5**
8	Explain about instruction cycle with flow chart?	**5**	**5**
9	Discuss different types of addressing modes with examples?	**5**	**5**
10	Explain about Design of control unit with neat diagram?	**5**	**5**
11	12. a) Explain about datatypes b) what is meant by fixed-point representation with examples	**5**	**5**

MID-II QUESTIONS
COMPUTER ORGANIZATION

II - B.TECH- I-SEM -II MID EXAMINATIONS

Date: 07-01-23 **Time: 10:00AM to 11:30AM**

Subject: COA Branch: CSE, AI&ML, IT, CS
Max. Marks: 25 M

Note: Question paper contains two parts, Part - A and Part - B.
Part-A is compulsory which carries 10 marks. Answer all questions in part-A.
Part-B consists of (2.5) units. Answer any one full question from each unit.
Each question carries 5 marks.

PART-A **5x 2M =10 M**

		BTL	CO
1.	Distinguish between RISC and CISC.	1	5
2.	What is cache coherence problem.	1	5
3.	Explain priority interrupt.	2	4
4.	Define cache hit and cache miss.	1	4
5.	What is the Handshaking mechanism?	1	4

PART-B **4 x 5 M = 20 M**

		BTL	CO
6.	Explain Booth's algorithm for multiplication with an example.	2	3
7.	Describe the following		

a. Associate memory 1 4

b. Decimal arithmetic operations 1 3

8. What are the different modes of data transfer? Explain each mode in detail. 2 4

9. Explain vector processing and array processor in detail with a neat diagram. 2 5

10. What is pipelining? Explain arithmetic and instruction pipeline. 2 5

11. Explain Floating – point addition /subtraction Algorithm with a flowchart. 2 3

Scheme of Evaluation

PART-A

S.NO.	THEORY	MARKS	TOTAL
1	Distinguish between RISC and CISC.	**2**	**2**
2	What is cache coherence problem.	**2**	**2**
3	Explain priority interrupt.	**2**	**2**
4	Define cache hit and cache miss.	**2**	**2**
5	What is the Handshaking mechanism?	**2**	**2**

PART-B

S.NO.	THEORY	MARKS	TOTAL
6	Explain Booth's algorithm for multiplication with an example.	5	5
7	Describe the following i)Associate memory ii) Decimal arithmetic operations	5	5
8	What are the different modes of data transfer? Explain each mode in detail.	5	5
9	What is pipelining? Explain arithmetic and instruction pipeline.	5	5
10	Explain Floating – point addition /subtraction	5	5

	Algorithm with a flowchart.		

12. Mapping of COs with POs and PSOs

COURSE CO-PO &PSO MATRIX	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	2	-	**1**	-	-	-	-	-	-	-	1	1	-
CO2	3	2	3	2	**2**	-	-	-	-	-	**1**	1	**2**
CO3	3	3	3	2	**2**	-	-	-	-	-	**2**	2	**2**
CO4	2	1	2	1	**2**	-	-	-	-	-	**1**	1	**1**
CO5	3	3	3	3	**3**	**1**	-	-	-	-	**3**	3	**3**
Average													

13. COs, POs, PSOs Justification

CO1.: Define the basic components of a digital computer. Understand the basics of micro-operations and the architecture of modern computers.
Correlated with PO1 medium: Because it contributes the knowledge on fundamentals of components of a digital computer which makes students acquire engineering knowledge.
Correlated with PO3 low: Because it develops the knowledge to identify the architecture of modern computers.
Correlated with PO11 low: Because it demonstrates knowledge, understanding and life-long learning in the broadest context of technological change.
Correlated with PSO1 low: Because it develops the ability to analyze the basics of digital computers and the architecture of modern computers.
CO2.: Describe arithmetic logic and shift micro-operations in symbolic form at a register transfer level. Develop the assembly language programming and demonstrate the addressing modes used in instructions.
Correlated with PO1high: Because it provides fundamentals of computer science. So, the correlation is good.
Correlated with PO2 moderately: Because it Apply preprocessing methods for any given raw data. So, correlation is good.

Correlated with PO3 High: Because it analyze complex engineering problems reaching substantiated conclusions.
Correlated with PO4 moderately: Because it helps to design solutions for complex engineering problems.
Correlated with PO5 moderately: Because it Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools.
Correlated with PO11 low: Because it demonstrates knowledge, understanding and life-long learning in the broadest context of technological change.
Correlated with PSO1 low : Because it helps in design and develop applications in assembly language.
Correlated with PSO2 moderately: Because it renders applications of Computing.
CO3.: Apply algorithm for arithmetic operations and implementations of ALU design.
Correlated with PO1 high: Because it provides an engineering specialization to the solution of complex engineering problems. So, the correlation is good.
Correlated with PO2 high: Because it provides an ability to analyze a problem, and identify and formulate the computing requirements appropriate to its solution.
Correlated with PO3 high: Because it provides design solutions for complex engineering problems.
Correlated with PO4 moderately: Because it conducts investigations of complex problems.
Correlated with PO5 moderately: Because it creates, selects, and applies appropriate techniques.
Correlated with PO11 moderately: Because it demonstrates knowledge, understanding and life-long learning in the broadest context of technological change.
Correlated with PSO1 moderately: Because it helps in design and develop applications in assembly language.
Correlated with PSO2 moderately: Because it renders applications of Computing.
CO4.: Understand the concepts of memory hierarchy and organization.
Correlated with PO1 moderately: Because it provides an engineering specialization to the solution of complex engineering problems.
Correlated with PO2 low: Because it provides an ability to analyze a problem, and identify and formulate the computing requirements appropriate to its solution.

Correlated with PO3 moderately: Because it provides design solutions for complex engineering problems.
Correlated with PO4 low: Because it conducts investigations of complex problems.
Correlated with PO5 moderately: Because it creates, selects, and applies appropriate techniques.
Correlated with PO11 low: Because it demonstrates knowledge, understanding and life-long learning in the broadest context of technological change.
Correlated with PSO1 low: Because it helps in design and develop applications in assembly language.
Correlated with PSO2 low: Because it renders applications of Computing.

CO5: Recognize the concepts of parallel processing, pipelining, and inter-processor communication. Design 3 and 4-stage pipeline processor.
Correlated with PO1 high: Because it provides an engineering specialization to the solution of complex engineering problems.
Correlated with PO2 high: Because it provides an ability to analyze a problem, and identify and formulate the computing requirements appropriate to its solutions.
Correlated with PO3 high: Because it provides design solutions for complex engineering problems.
Correlated with PO4 high: Because it conducts investigations of complex problems.
Correlated with PO5 high: Because it creates, selects, and applies appropriate techniques.
Correlated with PO6 low: Because it apply reasoning informed by the contextual knowledge.
Correlated with PO11 low: Because it demonstrates knowledge, understanding and life-long learning in the broadest context of technological change.
Correlated with PSO1 high: Because it helps in design and develop applications in assembly language.
Correlated with PSO1 high: Because it renders applications of Computing.

14. Attainment of CO's, PO's and PSO's (Excel Sheet)
(After Result)

15. University Question Papers/ Question Bank

Code No.: CS302PC | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Supply) - August- 2023
COMPUTER ORGANIZATION AND ARCHITECTURE
(Common to CSE, IT, CSC & CSM)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a)	Draw the Block diagram of a Digital Computer and Determine the importance of Digital Devices in modern era.	[2M]
b)	Discuss the Applications of Logic Micro Operations.	[2M]
c)	Define the i. Micro Operation ii. Micro Instruction iii. Micro Program iv. Micro Code.	[2M]
d)	Evaluate X= (A+B)*(C+D) and Describe the Zero address instruction.	[2M]
e)	Calculate the Binary and Octal value for $(2653)_{10}$	[2M]
f)	Convert the following Decimal number to the base indicated i. 17562 to Octal ii. 11938 to Hexadecimal	[2M]
g)	Explain the IEEE Representation of Floating point numbers.	[2M]
h)	Find 2's complement of $(101011)_2$.	[2M]
i)	Define Mapping and List different types of Mapping Techniques.	[2M]
j)	List the three Cache Memory mapping techniques.	[2M]

PART-B **(50 Marks)**

2.a)	Describe Memory Reference Instruction.	[5M]
b)	Explain the Common Bus System.	[5M]
	OR	
3.a)	Discuss and Explain Instruction Cycle with a neat sketch.	[5M]
b)	Classify and Explain the Computer Instructions.	[5M]
4.a)	Construct circuit for Program Control Status bit condition.	[5M]
b)	Explain the functioning of a Micro Program Sequencer.	[5M]
	OR	
5.	Evaluate X= (A+B)*(C+D) using 3 address, 2 address, 1 address and 0 address instruction formats.	[10M]
6.	Explain Addition and Subtraction Algorithm with a flowchart.	[10M]
	OR	
7.	Evaluate the following: • 6-9 • 12+8 • 5-(-3) by using binary.	[10M]
8.a)	Distinguish Static and Dynamic RAM chips.	[[5M]
b)	Distinguish Programmed I/O and Interrupt Initiated I/O modes of Data Transfer.	[5M]
	OR	
9.	Describe IOP-CPU-IOP Communication with a neat diagram.	[10M]
10.	Explain Concept of Pipelining in detail.	[10M]
	OR	
11.a)	Differentiate RISC and CISC characteristics.	[5M]
b)	Explain Cache Coherence.	[5M]

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Code No.: CS302PC | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
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COMPUTER ORGANIZATION AND ARCHITECTURE
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[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a)	Draw the Block diagram of a Digital Computer and Determine the importance of Digital Devices in modern era.	[2M]
b)	Discuss the Applications of Logic Micro Operations.	[2M]
c)	Define the i. Micro Operation ii. Micro Instruction iii. Micro Program iv. Micro Code.	[2M]
d)	Evaluate X= (A+B)*(C+D) and Describe the Zero address instruction.	[2M]
e)	Calculate the Binary and Octal value for $(2653)_{10}$	[2M]
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i)	Define Mapping and List different types of Mapping Techniques.	[2M]
j)	List the three Cache Memory mapping techniques.	[2M]

PART-B **(50 Marks)**

2.a)	Describe Memory Reference Instruction.	[5M]
b)	Explain the Common Bus System.	[5M]
	OR	
3.a)	Discuss and Explain Instruction Cycle with a neat sketch.	[5M]
b)	Classify and Explain the Computer Instructions.	[5M]
4.a)	Construct circuit for Program Control Status bit condition.	[5M]
b)	Explain the functioning of a Micro Program Sequencer.	[5M]
	OR	
5.	Evaluate X= (A+B)*(C+D) using 3 address, 2 address, 1 address and 0 address instruction formats.	[10M]
6.	Explain Addition and Subtraction Algorithm with a flowchart.	[10M]
	OR	
7.	Evaluate the following: • 6-9 • 12+8 • 5-(-3) by using binary.	[10M]
8.a)	Distinguish Static and Dynamic RAM chips.	[[5M]
b)	Distinguish Programmed I/O and Interrupt Initiated I/O modes of Data Transfer.	[5M]
	OR	
9.	Describe IOP-CPU-IOP Communication with a neat diagram.	[10M]
10.	Explain Concept of Pipelining in detail.	[10M]
	OR	
11.a)	Differentiate RISC and CISC characteristics.	[5M]
b)	Explain Cache Coherence.	[5M]

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16. Powerpoint presentations (PPTs)

Unit no	Topic name	Link
1	Instruction code	https://www.youtube.com/watch?v=mEw09EJwj30
1	Instruction cycle	https://www.youtube.com/watch?v=SFsnysyVhzA
1	Microprogrammed control unit	https://www.youtube.com/watch?v=81v7JqLbTMI http://www.infocobuild.com/education/audio-video-courses/computer-science/ComputerOrganization-IIT-Madras/lecture-07.html
2	Architecture of 8086	https://www.youtube.com/watch?v=CEL-jT4qFCk
2	Addressing modes of 8086	https://www.youtube.com/watch?v=hVRtfcvt1ns
2	Instruction set of 8086	https://www.youtube.com/watch?v=V3AeSmlZzw8
3	Interrupts of 8086	https://www.youtube.com/watch?v=LUVJxy-pGlM
3	Procedures and macros	https://www.youtube.com/watch?v=ybz0MYyum5M
3	Stack structure of 8086	https://www.youtube.com/watch?v=t35b-8w4Yrg
4	Computer arthimatic (addition , substraction)	https://www.youtube.com/watch?v=o-WXqnagg0c
4	Floating point arthimatic (addition)	https://www.youtube.com/watch?v=KiWz-mGFqHI
4	Asynchronous data transfer	https://www.youtube.com/watch?v=EzEqUH93C4U
5	Memory organization	https://www.youtube.com/watch?v=z_dSASDYc6c
5	Pipelining	https://www.youtube.com/watch?v=hGjX1Iw9Qxw
5	Multiprocessors	https://www.youtube.com/watch?v=fG3pmE2iRzo

17. Innovative Teaching method if any (Attached Innovative Assignment)

QUESTIONS

Q1. Explain the role of AI in future computer architecture.

Q2. Discuss about Edge computing.

Q3. Draw a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks.

Q4. What is an imprecise exception? State two possibilities of imprecise exception.

18. References (Textbook/Websites/Journals)

Textbooks

1. **Computer Organization** – Car Hamacher, Zvonks Vranesic, Safea Zaky, Vth Edition, McGraw Hill.
2. **Computer Organization and Architecture** – William Stallings Sixth Edition, Pearson/PHI.
3. **Structured Computer Organization** – Andrew S. Tanenbaum, 4th Edition, PHI/Pearson.

Websites/URLs/e-Resources

- www.wiley.com
- www.faadooengineers.com
- www.scribd.com
- www.slideshare.net
- www.google.com/co
- www.bookadda.com
- http://www.infocobuild.com