A

Course File Report

On

ANALOG AND DIGITAL ELECTRONICS (EC403ES)

Submitted by

Mr. G.PRAVALIKA
Assistant Professor , ECE Department

In the Department of
Computer Science & Engineering (CSE)

CMR ENGINEERING COLLEGE
(Approved by AICTE-New Delhi, Affiliated to J.N.T.U, Hyderabad)
Kandlakoya (v), Medchal Road, Hyderabad-501 401, Telangana State, India .Website: www.cmrec.ac.in
(2023-24)

CONTENTS OF COURSE FILE:

1. Department vision & mission
2. List of PEOs, POs, PSOs
3. List of Cos (action verbs as per blooms)
4. Syllabus copy and suggested or reference books
5. Individual Time table
6. Session plan/ lesson plan
7. Session execution log
8. Lecture notes
9. Assignment Questions along with sample assignment
10. Mid exam question papers along with sample answer scripts
11. Scheme of evaluation
12. Mapping of COs with POs and PSOs
13. Cos,Pos,PSOs justification
14. Attainment of COs with POs and PSOs
15. University question papers or question bank.
16. Power point presentations
17. Innovative teaching methods
18. References (Text book/Websites/Journals)

1. Department vision & mission

VISION

To accomplish an admirable standard of quality education by utilizing the latest technologies, innovations to be applicable for academia and industry which helps society in large.

MISSION

M1: To evolve professional who is proficient in the area of CSE

M2: To impart principle-based education and contribute to the innovation of computing and learning-based systems.

M3: Our Endeavour is to try new advancements in high-end computing hardware and software for society

2.List of PEOs, POs, PSOs

PROGRAM EDUCATIONAL OBJECTIVES (PEOS)

Programme educational objectives are broad statements that describe the career and professional accomplishments that the programme is preparing graduates to achieve within 3 to 5 years after graduation.

The **Programme Educational Objectives** of the B. Tech CSE programme are:

PEO1: To apply the knowledge of mathematics, basic science and engineering solving the real world computing problems to succeed higher education and professional careers.

PEO2: To develop the skills required to comprehend, analyze, design and create innovative computing products and solutions for real life problems.

PEO3: To inculcate professional and ethical attitude, communication and teamwork skills, multi-disciplinary approach and an ability to relate computer engineering issues with social awareness

PROGRAM OUTCOMES (POS)

Engineering Graduates will be able to satisfy these NBA graduate attributes:

1. **Engineering knowledge:** An ability to apply knowledge of computing, mathematics, science and engineering fundamentals appropriate to the discipline
2. **Problem analysis:** An ability to analyze a problem, and identify and formulate the computing requirements appropriate to its solution
3. **Design/development of solutions:** An ability to design, implement, and evaluate a computer-based system, process, component, or program to meet desired needs with appropriate consideration for public health and safety, cultural, societal and environmental considerations

4. **Conduct investigations of complex problems:** An ability to design and conduct experiments, as well as to analyze and interpret data

5. **Modern tool usage:** An ability to use current techniques, skills, and modern tools necessary for computing practice
6. **The engineer and society:** An ability to analyze the local and global impact of computing on individuals, organizations, and society
7. **Environment and sustainability:** Knowledge of contemporary issues
8. **Ethics:** An understanding of professional, ethical, legal, security and social issues and responsibilities
9. **Individual and team work:** An ability to function effectively individually and on teams, including diverse and multidisciplinary, to accomplish a common goal
10. **Communication:** An ability to communicate effectively with a range of audiences
11. **Project management and finance:** An understanding of engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects
12. **Life-long learning:** Recognition of the need for and an ability to engage in continuing professional development

PROGRAM SPECIFIC OUTCOMES (PSO'S)

1. **Professional Skills and Foundations of Software development:** Ability to analyze, design and develop applications by adopting the dynamic nature of Software developments
2. **Applications of Computing and Research Ability:** Ability to use knowledge in cutting edge technologies in identifying research gaps and to render solutions with innovative ideas

3. List of COs (action verbs as per blooms)

CO.1	• Know the characteristics of various components.
CO.2	• Understand the utilization of components.
CO.3	• Design and analyze small signal amplifier circuits.
CO.4	• Learn Postulates of Boolean algebra and to minimize combinational functions
CO.5	• Design and analyze combinational and sequential circuits
CO.6	• Know about the logic families and realization of logic gates

4. Syllabus copy and suggested or reference books

UNIT - I

Diodes and Applications: Junction diode characteristics: Open circuited p-n junction, p-n junction as a rectifier, V-I characteristics, effect of temperature, diode resistance, diffusion capacitance, diode switching times, breakdown diodes, Tunnel diodes, photo diode, LED.

Diode Applications - clipping circuits, comparators, Half wave rectifier, Full wave rectifier, rectifier with capacitor filter.

UNIT - II

BJTs: Transistor characteristics: The junction transistor, transistor as an amplifier, CB, CE, CC configurations, comparison of transistor configurations, the operating point, self-bias or Emitter bias, bias compensation, thermal runaway and stability, transistor at low frequencies, CE amplifier response, gain bandwidth product, Emitter follower, RC coupled amplifier, two cascaded CE and multi stage CE amplifiers.

UNIT - III

FETs and Digital Circuits: FETs: JFET, V-I characteristics, MOSFET, low frequency CS and CD amplifiers, CS and CD amplifiers.

Digital Circuits: Digital (binary) operations of a system, OR gate, AND gate, NOT, EXCLUSIVE OR gate, De Morgan Laws, NAND and NOR DTL gates, modified DTL gates, HTL and TTL gates, output stages, RTL and DCTL, CMOS, Comparison of logic families.

UNIT - IV

Combinational Logic Circuits: Basic Theorems and Properties of Boolean Algebra, Canonical and Standard Forms, Digital Logic Gates, The Map Method, Product-of-Sums Simplification, Don't-Care Conditions, NAND and NOR Implementation, Exclusive-OR Function, Binary Adder-Subtractor, Decimal Adder, Binary Multiplier, Magnitude Comparator, Decoders, Encoders, Multiplexers.

UNIT - V

Sequential Logic Circuits: Sequential Circuits, Storage Elements: Latches and flip flops, Analysis of Clocked Sequential Circuits, State Reduction and Assignment, Shift Registers, Ripple Counters, Synchronous Counters, Random-Access Memory, Read-Only Memory

TEXT BOOKS:

1. Integrated Electronics: Analog and Digital Circuits and Systems, 2/e, Jaccob Millman, Christos Halkias and Chethan D. Parikh, Tata McGraw-Hill Education, India, 2010.
2. Digital Design, 5/e, Morris Mano and Michael D. Cilette, Pearson, 2011.

REFERENCE BOOKS:

1. Electronic Devices and Circuits, Jimmy J Cathey, Schaum's outline series, 1988.

2. Digital Principles, 3/e, Roger L. Tokheim, Schaum's outline series, 1994

5. Individual Time Table

	I	II	III	IV		V	VI	VII
MON			CSE –A LAB					CSE-A
TUES	CSE-C	CSE-A					CSE-C	
WED	CSE-A			CSE-C			CSE –C LAB	
THUR								
FRI		CSE-A					CSE –A LAB	
SAT			CSE –C LAB			CSE-A		CSE-C

6. Session plan/ lesson plan

S.NO	TOPIC TO BE COVERED	Suggested Books (Eg: T1,T2,)	NO. OF LECTURES REQUIRED	Teaching methods
	UNIT-I Classes required – 12			
1	Introduction	T1,R1	1	White board, PPT
2	Junction diode characteristics: Open circuited p-n junction,:	T1	1	White board, PPT
3	V-I characteristics	T1,R1	1	White board, PPT
4	Effect of temperature, diode resistance, diffusion capacitance	T1	2	White board, PPT
5	diode switching times	T1,R1	1	White board, PPT
6	Breakdown diodes ,Tunnel diodes, photo diode, LED	T1	1	White board, PPT
7	Diode Applications - clipping circuits	T1,R1	1	White board, PPT
8	Comparators	T1	1	White board, PPT

9	Half wave rectifier, Full wave rectifier	**T1**	**2**	**White board, PPT**
10	capacitor filter	**T1**	**1**	**White board, PPT**
Unit-II Classes required-13				
11	**BJTs**: Transistor characteristics: The junction transistor	**T1,R1**	**2**	**White board, PPT**
12	transistor as an amplifier	**T1**	**2**	**White board, PPT**
13	CB configurations, CE configurations	**T1**	**1**	**White board, PPT**
14	CC configurations, comparison of transistor configurations	**T1**	**1**	**White board, PPT**
15	the operating point, self-bias or Emitter bias, bias compensation	**T1**	**1**	**White board, PPT**
16	Thermal runaway and stability	**T1**	**1**	**White board, PPT**
17	Transistor at low frequencies, CE amplifier Response	**T1**	**1**	**White board, PPT**
18	Gain bandwidth product	**T1**	**1**	**White board, PPT**
19	Emitter follower, RC coupled amplifier	**T1**	**2**	**White board, PPT**
20	two cascaded CE and multi stage CE amplifiers	**T1**	**1**	**White board, PPT**
UNIT-III Classes required – 10				
21	**FETs and Digital Circuits**: FETs: JFET, V-I characteristics	**T1**	**1**	**White board, PPT**
22	MOSFET	**T1**	**1**	**White board, PPT**
23	low frequency CS and CDamplifiers	**T1**	**1**	**White board, PPT**

24	Digital Circuits: Digital (binary) operations of a system,	**T1**	**1**	**White board, PPT**
25	OR gate, AND gate, NOT, EXCLUSIVE OR Gate	**T1**	**1**	**White board, PPT**
26	De Morgan Laws	**T1**	**1**	**White board, PPT**
27	NAND and NOR DTL gates	**T1**	**1**	**White board, PPT**
28	modified DTL gates	**T1**	**1**	**White board, PPT**
29	HTL and TTL gates output stages, RTL and DCTL,	**T1**	**1**	**White board, PPT**
30	CMOS, Comparison of logic families	**T1**	**1**	**White board, PPT**
UNIT-IV Classes required – 10				
31	**Combinational Logic Circuits:** Basic Theorems and Properties of Boolean Algebra,	**T2**	**1**	**White board, PPT**
32	Canonical and Standard Forms, Digital Logic Gates	**T2**	**1**	**White board, PPT**
33	The Map Method, Product-of-Sums Simplification, Don't-Care Conditions	**T2**	**1**	**White board, PPT**
34	NAND and NOR Implementation	**T2**	**2**	**White board, PPT**
35	Exclusive-OR Function	**T2**	**1**	**White board, PPT**
36	Binary Adder-Subtractor, Decimal Adder	**T2**	**1**	**White board, PPT**
37	Binary Multiplier	**T2**	**1**	**White board, PPT**
38	Magnitude Comparator	**T2**	**1**	**White board, PPT**
39	Decoders, Encoders, Multiplexers	**T2**	**2**	**White board, PPT**

UNIT-V Classes required – 12				
40	**Sequential Logic Circuits:** Sequential Circuits,	**T2**	1	**White board, PPT**
41	Storage Elements: Latches and flip flops	**T2**	2	**White board, PPT**
42	Analysis of Clocked Sequential Circuits	**T2**	1	**White board, PPT**
43	State Reduction and Assignment	**T2**	2	**White board, PPT**
44	Shift Registers	**T2**	2	**White board, PPT**
45	Ripple Counters	**T2**	2	**White board, PPT**
46	Synchronous Counters	**T2**	2	**White board, PPT**
Total no of classes : 57				

7. Session execution log

S NO	UNIT	SCHEDULED COMPLETED DATE	COMPLETED DATE	REMARKS
1	**I**	19.02.2024	08.03.2024	Completed
2	**II**	11.03.2024	31.03.2024	Completed
3	**III**	01.04.2024	24.04.2024	Completed
4	**IV**	26.05.2024	05.06.2024	Completed
5	**V**	10.06.2024	29.06.2024	Completed

8. Lecture notes

ADE NOTES.zip

9. Assignment Questions along with sample assignment

II.B.TECH- II-SEM –I MID EXAMINATIONS, ASSIGMENT TEST

Subject: ADE **Branch: CSE Session:B&D** **Marks: 5M**

Answer all questions. **5*1=5**

1. (a)Comparison of CB,CC and CE configurations?

   (b)Derive the relation between α, β, γ

2.(a) Explain the operation of operating point of a transistor?

   (b).Explain the operation of NPN and PNP transistor ?

3. (a) Explain the operation of Multistage CE amplifier circuit?

   (b) Define self bias? Derive the expression stability factor for self bias ?

4. Explain the input and output characteristics of a transistor in CE configuration?

5. Explain the input and output characteristics of a transistor in CB configuration?

II.B.TECH- II-SEM II MID EXAMINATIONS

Subject: ADE **Branch: CSE (B,D)** **Marks:05M**

ASSIGNMENT QUESTIONS

ANSWER ANY FIVE QUESTIONS

1.(a) Draw the logic circuit of a 16* 4 encoder with 4*2 and 8*3 and explain its working? **[CO-6] [BTL -5]**

(b) Explain the operation of TTL with neat diagram.? **[CO-5] [BTL -3]**

2. (a) Draw and explain SR flip flop with truth table and find characteristics equation? **[CO-6] [BTL -5]**

(b) Draw and Explain the logic diagram of 4 bit ring counter with the help of timing diagrams.? **[CO-6] [BTL-3]**

3.(a) Explain the operation NAND and NOR DTL gates ? **[CO-5] [BTL -3]**

(b) Design the 4-bit binary Adder-Subtractor with suitable diagram.? **[CO-5] [BTL -3]**

4. (a) Realise D-FF and T-FF using JK FF? **[CO-6] [BTL -4]**

(b) Design a modulo 10 counter using JK flipflops and explain its timing diagram? **[CO-6] [BTL -4]**

5.(a) Explain the design procedure of clocked synchronous sequential circuits? **[CO-6] [BTL -3]**

(b) Simplify the following function using K-map. F(A,B,C,D) = πM(1,3,4,5,6,11,13,14,15) **[CO-5] [BTL-3]**

6. Explain the operation of all types shift register ? **[CO-6] [BTL -3]**

7. Minimise the following Boolean function using K-map and design a logic circuit using NAND gates. F=Σm (1,5,6,12,13,14)+d(2,4) **[CO-5] [BTL -3]**

10. Mid exam question papers along with sample answer scripts.

CMR ENGINEERING COLLEGE
UGC AUTONOMOUS
(Approved by AICTE - New Delhi. Affiliated to JNTUH and Accredited by NAAC & NBA)
Kandlakoya (V), Medchal (M), Medchal - Malkajgiri (D)-501401

II.B.TECH- II-SEM –I MID EXAMINATIONS ***Date:*** **18.04.2024** **Time:** ***01.00 PM TO 03.00 PM***

Subject: ADE (R22EC403ES) **Branch:CSE,** **Marks: 30M**

Note: Question paper contains two parts,Part - A and Part - B.

Part-A is compulsory which carries 10 marks. Answer all questions in part-A.
Part-B. Answer any FOUR questions out of SIX qustions (4*5=20 MARKS)

PART-A

5x2=10

1.	What is the effect of temperature on diode?	**CO.1 [BTL-1]**
2.	Define biased clipper and draw its output wave forms?	**CO.1 [BTL-1]**
3.	What is thermal runaway ?	**CO.2 [BTL-1]**
4.	Describe how transistor act as an amplifier?	**CO.2 [BTL-1]**
5.	Explain FET?	**CO.2 [BTL-2]**

PART-B

4X5=20

6. Discuss the different types of junction breakdowns that can occur in a reverse biased diode. **CO.2 [BTL-4]**
7. Explain the operation full wave rectifier with and without filters? **CO.2 [BTL-3]**
8 Explain the input and output characteristics of a transistor in CE configuration. **CO.2 [BTL-2]**
9. Draw and explain the V-I characteristics of a tunnel diode? **CO.1 [BTL-2]**
10. Explain the operation of operating point of a transistor? **CO.2 [BTL-2]**
11. Explain the operation of NPN transistor? **CO.3 [BTL-2]**

II.B.TECH- II-SEM -II MID EXAMINATIONS ***Date:*** **03.07.2024** **Time*: 01.30PM-03.30PM***

Subject: ADE ADE(R22EC403ES) **Branch: CSE,CSC** **Marks: 30M**

Note: Question paper contains two parts, Part - A and Part - B.
Part-A is compulsory which carries 10 marks. Answer all questions in part-A.
Part-B consists of (2 1/2) units. Answer any one full question from each unit. Each question carries 5 marks and may have a,b,c sub questions.

PART-A

5x2=10

		BTL	CO
1.	Explain magnitude comparator ?	4	6
2.	Difference between Latches and Filpflops?	4	5
3.	Define multiplexer and Draw 4*1 mulipleaxer logic diagram?	4	3
4.	What is an electronic gates and what are they?	5	3
5.	Explain the different types of ROM?	1	6

PART-B

4X5=20

		BTL	CO
6.	Minimize the following expressions using K-map $F = \sum m(1, 3,7,11,15) + d(0,2,5)$ $Y = \pi M(4,5,6,7,8,12)\ .d(1,2,3,9,11,14)$	3	4
7.	Explain the 16*4 encoder with 4*2 and 8*3 encoder	2	4
8	Design a modulo 10 counter using JK flipflops and explain its timing diagram	3	4
9.	Using D Flip flop and waveforms , Explain the working of a 4-bit PISO shift register?	4	6
10.	Explain the logic family RTL and DCTL gates ?	3	6
11.	Explain the operation NAND and NOR with modified DTL gates?	6	5

11.SCHEME OF EVALUATION:

PART	S.NO	QUESTIONS	MARKS	TOTAL
A	1	How increases voltage and current with temperature changes	2	2
	2	Definition of biased clipper and draw its wave form	1 1	2
	3	Definition of thermal runaway	2	2
	4	Transistor act as an amplifier	2	2
	5	Defination FET Explain two lines about FET	1 1	2
B				
	6	Definition Breakdown Mechanism each 2 Marks	1 4	5
	7	Full wave rectifier definition and operation with and without filters	2 3	5
	8	Definition of CE transistor Input and Output Characteristics	1 4	5
	9	Defination of tunnel diode V-I characteristics of tunnel diode	1 4	5
	10	Definition of operating point of transistor and explain it	1 4	5
	11	Opearation of NPN transistor and find its current	3 2	5
				5

Scheme of Evaluation(MID-2)

S.No	Theory(Part-A)	Marks	Total
1	Defination magnitude comparator? Block diagram	2M	**2M**
2	Any two difference between Latches and Filpflops	2M	**2M**
3	Define multiplexer Draw 4*1 mulipleaxer logic diagram	1M 1M	**2M**
4	For definition an electronic gates Mentioned any two gates names and symbol	1M 1M	**2M**
5	Definition of ROM	1M	**2M**
	Mentioned different types	1M	
Total			**10M**

S.No	Theory(Part-B)	Marks	Total
6	Minimize the K map (a) $F = \sum m(1, 3,7,11,15) + d(0,2,5)$	2 1/2M	**5M**
	(b) $Y = \pi M(4,5,6,7,8,12) .d(1,2,3,9,11,14)$	2 1/2M	
7	Definition Encoder the 16*4 encoder with 4*2 and 8*3 encoder	1 M 4M	**5M**
8	Design a modulo 10 counter using JK flipflops and explain its timing diagram	5M	**5M**
9	Using D Flip flop and waveforms the working of a 4-bit PISO shift register	1M 4M	**5M**
10.	Defination RTL,DCTL Explanations the logic family RTL DCTL gates	2 M 1 ½ M 1 ½ M	**5M**
11.	the operation NAND modified DTL NOR with modified DTL gates	2 ½ M 2 ½ M	**5M**

12. Mapping of COs with POs and PSOs

COURSE CO-PO&PSO-MATRIX	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO10	PO11	PO12	PSO 1	PSO 2
CO1	3	3	3	-	2	-	-	-	-	-	-	1	1	-
CO2	3	3	3	3	3		-	-	-	-	-	1	1	1
CO3	3	3	3	2	2	2	-	-	-	-	-	1	1	-
CO4	3	3	3	2	2	2	-	-	-	-	-	1	1	1
CO5	3	3	3	2	2	2	-	-	-	-	-	1	1	-
C06	3	3	3	2	2	2	-	-	-	-	-	2	1	1
AVERAGE	**3**	**3**	**3**	**2**	**2**	**2**	**-**	**-**	**-**	**-**	**-**	**1**	**1**	**1**

13. Cos,Pos,PSOs justification

Justification for Correlation of CO-PO

CO1: Explain fundamentals of various components Diode,BJT,FET.resistor ,capacitor
Correlated with PO1 substantially: Because it deals with fundamentals of electronics how to deelop the components which makes students to acquire engineering knowledge.
Correlated with PO2 substantially: Because it provides students identify different diodes how to construct the types of diodes and working
Correlated with PO3 substantially: Because it makes students select the different types of Diode,BJT,FET introduce operation
Correlated with PO5 Moderately: Beacause it makes students select the different tools in diodes,photo diode ,led

CO2: Explain Understand the utilization of components
Correlated with PO1 substantially: Because it deals with fundamentals of electrical properties of diode circuits which makes students to acquire engineering knowledge.and where we can used rectifier ,switch,amplifier
Correlated with PO2 substantially: Because it makes students select appropriate didoe uses in the rectifier ,to knoe how the voltage stabilizer working.
Correlated with PO3 substantially: Because it makes students to select appropriate diodes and transistor in the usage in the different aspects
Correlated with PO4 substantially: Because it makes studnets to aspect the knowlwdge and understand uses in the engineering**.**

Correlated with PO5 substantially: Because it makes to students to draw the circuit in the another application

CO3: Design and analyze small signal amplifier circuits.
Correlated with PO1 substantially: Because it deals with fundamentals of analog electronics circuits which makes students to acquire engineering knowledge.
Correlated with PO2 substantially: Because itmakes students to draw amplifier circuits and analyze in tye complex in the research.
Correlated with PO3 substantially: Because itmakes students to draw the amplifier circuit design and bandwidth which uses in the different configurations circuits.
Correlated with PO4 moderately: Because it makes students to perform the operation small signal amplifier circuits in the mehod .
Correlated with PO5 moderately: Because it makes students to work as a team design the amplifier circuits .
Correlated with PO6 moderately: Because students have to adopt to method in the amplifier in the h parameters value in the circuits .

• **CO4: Learn** Postulates of Boolean algebra and to minimize combinational functions
Correlated with PO1 substantially: Because it deals with fundamentals of Boolean algebra and combinational functions acquire engineering knowledge.
Correlated with PO2 substantially: Because itmakes students to analyze characteristics of logic gates which contributes a solution to complex problems and review research.
Correlated with PO3 substantially: Because itmakes students to perform parametric analysis of logic gates which contributests design of combinational with minimizations circuits.
Correlated with PO4 modearately: Because itmakes students to perform minimizational of logic gates which contributesto design ofcombiantioanl circuits circuits
Correlated with PO5 modearately: Because it makes students to perform analysis of logic gates using bread board connection and execute .
Correlated with PO6 moderately: Because it makes students to work as a team while performing learning of Boolean algebra method to reduce digital circuits analysis.

• **CO5: Design** and **analyze** combinational and sequential circuits .
Correlated with PO1 substantially: Because it deals with fundamentals of combinatioal and sequential circuits which makes students to acquire engineering knowledge.
Correlated with PO2 substantially: Because it makes students to identify building blocks of combinatioanal and sequential circuits a solution to complex problems and review research.
Correlated with PO3 substantially: Because it makes students to design encoders,decoders,multiplexers and comparators which contributesto design of CMOS circuits.
Correlated with PO4 moderately: Because it makes students to interpret different types of combianrtioanl and sequential circuits design in the system.
Correlated with PO5substantially: Because it makes students to model building blocks of

combinational circuits and sequential circuits in the using bread board connection
Correlated with PO6 moderately: Because it makes students to build different digital systems using the a team.
• **CO6: Design** the logic families and realization of logic gates .
Correlated with PO1 substantially: Because it deals with fundamentals of logic families and logic gates which makes students to acquire engineering knowledge.
Correlated with PO2 substantially: Because it makes students to identify appropriate logic families with logic gates which contributes a solution to complex problems and review research.
Correlated with PO3 substantially: Because it makes students to design logic circuits using logic gates .
Correlated with PO4 moderately: Because it makes students to interpret programmable logic families DTL,RTL,CMOS in order to design logic circuits.
Correlated with PO5substantially: Because it makes students to prototype logic circuits using resistor,bread board tools.
Correlated with PO9 moderately: Because it makes students to work as a team in design of logic circuits using logic gates .
Correlated with PO12 moderately: Because students have to adopt to changes logic families with realization of logic gates.

Justification for Correlation of CO-PSO

CO1: Explain fundamentals of electronics in the analog input circuits circuits.
Correlated with PSO1 moderately: Because it makes students to apply fundamentals of electronics in the analog inputs .

CO2: Choose an appropriate diode and using electrical properties of analog circuits.
Correlated with PSO1 substantially: Because it deals with fundamentals of electrical properties of analog circuits which makes students to study analog circuits.
Correlated with PSO2 moderately: Because itmakes students select appropriate inverter which contributes to design of analog circuits.

CO3: Design and analyze small signal amplifier circuits
Correlated with PSO1 substantially: Because it deals with fundamentals of analog circuits which makes students to draw circuit diagram of analog diode and transistor circuits.
Correlated with PSO2 substantially: Because itmakes students to draw analog circuits which contributes to design of analog circuits.

• **CO4: Learn** Postulates of Boolean algebra and to minimize combinational functions

Correlated with PSO1 substantially: Because it deals with fundamentals of logic gateswhich makes students to interpret characteristics ofdigital circuits.
Correlated with PSO2 substantially: Because itmakes students to perform parametric analysis of logic gates which contributesto design of MOS circuits.

CO5: Design and analyze combinational and sequential circuits.
Correlated with PSO1 substantially: Because it deals with fundamentals of memorieswhich makes students to build data path.
Correlated with PSO2 substantially: Because itmakes students to design memories and building blocks of data path sub system which contributesto design of MOS circuits.

• **CO6: Design** about the logic families and realization of logic gates
Correlated with PSO1 substantially: Because it deals with fundamentals of programmable deviceswhich makes students to configure programmable devices.
Correlated with PSO2 substantially: Because it makes students to identify building blocks of combinatioanal and sequential circuits a solution to complex problems and review research.

14. Attainment of COs with POs and PSOs

Relationship of Course outcomes to Program Outcomes (PO AVG)													
PO1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO1 0**	**PO1 1**	**PO1 2**	**PSO 1**	**PSO 2**
2	2	1	-	-	-	1	3	1	2	-	-	-	1
-	3	2	1	-	2	-	-	-	-	-	-	1	2
1	3	3	2	-	-	2	-	-	-	-	-	1	3
1	2	3	-	-	-	-	-	2	-	-	-	-	1
-	2	1	-	-	2	-	-	-	3	-	-	-	-
1	-	2	2	-	-	3	-	-	-	-	1	-	2

ASSESSMENT OF POs THROUGH THE COURSE			
PO	**CO**	**Value**	**AVG PO (Mid)**
PO1	CO1		
	CO3		
	CO4		
	CO5		

	CO6		
PO2	CO1		
	CO2		
	CO3		
	CO4		
	CO5		
PO3	CO1		
	CO2		
	CO3		
	CO4		
	CO5		
	CO6		
PO4	CO2		
	CO3		
	CO6		
PO5	CO5		
PO12	CO2		
PSO1	CO2		
	CO3		
PSO2	CO1		
	CO2		
	CO3		
	CO4		
	CO6		

15.University question papers or question bank.

ADE QP PREVIOUS.zip

QUESTION BANK

ANALOG AND DIGITAL ELECTRONICS question bank.zip

16.Power point presentations

ade unit 1.zip

ade unit 2.zip

ADE 3 UNIT.zip

ade 4th unit.zip

ADE 5TH UNIT.zip

17. INNOVATIVE TEACHING METHODS

Student-Centric Focus

Innovative teaching strategies prioritize the needs and engagement of students, fostering active participation in the learning process.

Active Learning

Encourages hands-on and participatory activities, moving away from passive learning to promote deeper understanding and retention.

Flexibility and Adaptability

Adapts to the diverse learning styles and needs of students, offering flexibility in content delivery and new teaching methods.

Technology Integration

Utilizes technology creatively to enhance effective learning experiences, incorporating digital tools and resources for effective and interactive instruction.

Collaborative Learning

Emphasizes group work, collaboration, and peer learning to enhance social and communication skills among students.

Problem-Solving Emphasis

Focuses on developing critical thinking skills and problem-solving skills, challenging students to apply knowledge in real-world scenarios.

Continuous Assessment

Moves beyond traditional exams and grades by implementing continuous assessment methods, providing ongoing feedback for improvement.

Creativity Encouragement

Cultivates a learning environment that stimulates creativity and innovation, allowing students to express themselves and explore new ideas.

Individualized Learning Paths

Recognizes and accommodates the diverse learning preferences and paces of individual students, promoting personalized learning experiences.

Real-World Relevance

Connects classroom concepts to real-world applications, demonstrating the practical relevance of what students are learning.

Feedback-Oriented Approach

Prioritizes constructive feedback to guide students' progress, facilitating a continuous cycle of improvement and reflection.

18. References (Text book/Websites/Journals)

1. nptel.ac.in/courses/108/102/108102095/
2. nptel.ac.in/courses/108/105/108105132/
3. nptel.ac.in/courses/108/102/108102112/
4. www.geeksforgeeks.org/digital-electronics-logic-design-tutorials/
5. https://www.coursera.org/specializations/semiconductor-devices