A

Course File Report

On

"COMPUTER ORGANISATION & ARCHITECTURE"

Submitted by

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(2022-2023)

COURSE FILE

Subject: COMPUTER ORGANISATION & ARCHITECTURE

Year: II–B-TECH, I SEM **Branch: CSE**

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Submitted By
Y.SHYAM SUNDAR
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CSE Dept

1. Department vision & mission

Vision

- To be recognized as a premier institution in offering value based and futuristic quality technical education to meet the technological needs of the society

Mission

- To impart value based quality technical education through innovative teaching and learning methods
- To continuously produce employable technical graduates with advanced technical skills to meet the current and future technological needs of the society
- To prepare the graduates for higher learning with emphasis on academic and industrial research

2.1 Program Educational outcome (PEO):

- Excel in professional career or higher education by acquiring knowledge in mathematical, computing and engineering principles
- To provide intellectual environment for analyzing and designing computing systems for technical needs
- Exhibit professionalism, multidisciplinary teamwork and adapt to current trends by engaging in lifelong learning and practice their profession with legal, social and ethical responsibilities

2.2 Program Outcome (PO):

1. **Engineering knowledge:** An ability to apply knowledge of computing, mathematics, science and engineering fundamentals appropriate to the discipline
2. **Problem analysis:** An ability to analyze a problem, and identify and formulate the computing requirements appropriate to its solution

3. **Design/development of solutions:** An ability to design, implement, and evaluate a computer-based system, process, component, or program to meet desired needs with appropriate consideration for public health and safety, cultural, societal and environmental considerations
4. **Conduct investigations of complex problems:** An ability to design and conduct experiments, as well as to analyze and interpret data
5. **Modern tool usage:** An ability to use current techniques, skills, and modern tools necessary for computing practice
6. **The engineer and society:** An ability to analyze the local and global impact of computing on individuals, organizations, and society
7. **Environment and sustainability:** Knowledge of contemporary issues
8. **Ethics:** An understanding of professional, ethical, legal, security and social issues and responsibilities
9. **Individual and team work:** An ability to function effectively individually and on teams, including diverse and multidisciplinary, to accomplish a common goal
10. **Communication:** An ability to communicate effectively with a range of audiences
11. **Project management and finance:** An understanding of engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects
12. **Life-long learning:** Recognition of the need for and an ability to engage in continuing professional development

CO1	**Define** the basic components of a digital computer
CO2	**Design** of CPU, ALU and Control Unit.
CO3	**Illustrate** the Data types and arithmetic algorithms
CO4	**Analyze** Input output organization
CO5	**Determine** the memory hierarchy, parallelism and pipelining for high performance processor

3. List of COs (Action verbs as per Bloom's Taxonomy)

4. Syllabus

UNIT – I

Digital Computers: Introduction, Block diagram of Digital Computer, Definition of Computer Organization, Computer Design and Computer Architecture.

Register Transfer Language and Micro operations: Register Transfer language, Register Transfer, Bus and memory transfers, Arithmetic Micro operations, logic micro operations, shift micro operations, Arithmetic logic shift unit.

Basic Computer Organization and Design: Instruction codes, Computer Registers Computer Instructions, Timing and Control, Instruction cycle, Memory Reference Instructions, Input – Output and Interrupt.

UNIT – II

Micro programmed Control: Control memory, Address sequencing, micro program example, design of control unit.
Central Processing Unit: General Register Organization, Instruction Formats, Addressing modes, Data Transfer and Manipulation, Program Control.

UNIT – III

Data Representation: Data types, Complements, Fixed Point Representation, Floating Point Representation.
Computer Arithmetic: Addition and subtraction, multiplication Algorithms, Division Algorithms, Floating – point Arithmetic operations. Decimal Arithmetic unit, Decimal Arithmetic operations.

UNIT – IV

Input-Output Organization: Input-Output Interface, Asynchronous data transfer, Modes of Transfer, Priority Interrupt Direct memory Access.
Memory Organization: Memory Hierarchy, Main Memory, Auxiliary memory, Associate Memory, Cache Memory.
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UNIT – V

Reduced Instruction Set Computer: CISC Characteristics, RISC Characteristics.
Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processor.
Multi Processors: Characteristics of Multiprocessors, Interconnection Structures, Interprocessor Arbitration, Interprocessor communication and synchronization, Cache Coherence.

TEXT BOOK:

1. **Computer System Architecture** – M. Moris Mano, Third Edition, Pearson/PHI.

REFERENCES:

1. **Computer Organization** – Car Hamacher, Zvonks Vranesic, Safea Zaky, Vth Edition, McGraw Hill.
2. **Computer Organization and Architecture** – William Stallings Sixth Edition, Pearson/PHI.
3. **Structured Computer Organization** – Andrew S. Tanenbaum, 4th Edition, PHI/Pearson.

5. Session Plan/Lesson Plan

S.No	Topic(JNTU syllabus)	Sub-Topic	No. Of Lectures Required	Suggested Books	Remarks
1	**UNIT-I** **Digital Computer, Register Transfer Language And Micro operations, Basic Computer Organization And Design**	Introduction, Block diagram of Digital Computer	L1	T1	
2		Definition of Computer Organization, Computer Design and Computer Architecture.	L2	T1	
3		Instruction codes	L3	T1	
4		Computer Registers	L4	T1	
5		Computer instructions	L5	T1	
6		Timing and Control	L6	T1	
7		Instruction cycle	L7	T1	
8		Memory Reference Instructions	L8	T1	
9		Input – Output and Interrupt	L9	T1	
10		Complete Computer Description	L10	T1	
11	**UNIT - II** **Micro Programmed Control, CPU**	Control memory	L11	T2	
12		Address sequencing	L12	T2	
13		micro program example	L13	T2	
14		General Register Organization	L14	T2	
15		Instruction Formats	L15	T2	

16		Addressing modes	L16	T2	
17		Data Transfer and Manipulation	L17	T2	
		Program Control.	L18	T2	
18		design of control unit	L19	T2	
19	**UNIT - III** **Data Representation , Computer Arithmetic**	Data Types	L20	T2	
20		Complements	L21	T2	
21		Fixed Point Representation	L22	T2	
22		Floating Point Representation.	L23	T2	
23		Addition And Subtraction	L24	T2	
24		Multiplication Algorithms	L25	T2	
25		Division Algorithms	L26	T2	
26		Floating – Point Arithmetic Operations.	L27	T2	
27		Decimal Arithmetic Unit	L28	T2	
28		Decimal Arithmetic Operations.	L29	T2	
30	**UNIT-IV** **I/O Organization, Memory Organization**	Peripheral Devices	L30	T1	
31		Input-Output Interface	L31	T1	
32		Asynchronous Data Transfer	L32	T1	
33		Modes Of Transfer	L33	T1	
34		Priority Interrupt	L34	T1	
35		Direct Memory Access	L35	T1	
36		Input –Output Processor (Iop)	L36	T1	
37		Memory Hierarchy	L37	T1	
38		Main Memory	L38	T1	

39		Auxiliary Memory	L39	T1	
40		Associate Memory	L40	T1	
41		Cache Memory	L41	T1	
42	**UNIT-V** **RISC, Pipeline And Vector Processing , Multiprocessor**				
42		SISC AND RISC	L41	T1	
43		Parallel Processing	L42	T1	
44		Pipelining, Arithmetic Pipeline	L43	T1	
45		Instruction Pipeline	L44	T1	
46		Risc Pipeline	L45	T1	
47		Vector Processing,	L46	T1	
48		Characteristics Of Multiprocessors	L47	T1	
49		Interconnection Structures	L48	T1	
50		Interprocessor Arbitration	L49	T1	
51		Array Processors	L50	T1	
52		Inter Processor Communication, And Synchronization	L51	T1	

6. Session execution log

S no	Unit	Scheduled completed date	Completed date	Remarks
1	**I**	10-10-22	25-10-22	COMPLETED
2	**II**	25-10-22	19-11-22	COMPLETED
3	**III**	23-11-22	22-12-22	COMPLETED
4	**IV**	26-12-22	10-1-23	COMPLETED
5	**V**	11-1-23	26-1-23	COMPLETED

7. Lecture Notes

8. Assignment Questions along with sample Assignments Scripts

ASSIGNMENT QUESTIONS

MID-I

1 (a) Explain about Block Diagram of Digital computer.
(b) Difference between Computer Organization &Architecture.
2 (a) Explain about Micro Operations.
(b) Define Micro operations and explain various types of micro operations with example.
3 (a) Draw arithmetic logic shift unit and explain.
(b) Discuss computer registers and computer instructions.
4 Explain about Instruction format and Instruction cycle.
5 (a) Explain about addressing modes
(b) Explain about Address sequencing

MID-II

1) a) Explain Addition and Subtraction Algorithm with Example and Neat Diagram?
b) I) Explain Multiplication Algorithm with Example's?
II) Describe Booth Multiplication with Example?
2) a) Explain Division Algorithm with Example?
b) Write about Decimal Arithmetic unit and Decimal Arithmetic operations with Example?
3) a) Discuss about Input-Output Interface with neat diagram?
b) Write about Asynchronous Data Transfer and Modes of Transfers?
4) a) Explain about Memory Hierarchy with neat diagram?
b) Explain about Associative Memory with neat diagram?
5) a) Distinguish CISC and RISC characteristics?
b) Explain types of Pipeline and Vector Processing?

9. Mid exam Question Papers along with sample Answers Scripts

A.Y 2022-23

MID-I QUESTION PAPER

COMPUTER ORGANISATION AND ARCHITECTURE

B.TECH-II

I-MIDEXAMINATIONS

Date: Time: 10:00AMto11:30AM

Subject: C O A **Branch: CSE/IT/AIML**

Note: Question paper contains two parts, Part-A and Part- B.

Part-A is compulsory which carries 10 marks. Answer all questions in part-A.

Part-B Answer anyone full question from each unit. Each question carries5 marks.

PART-A 5x2M =10 M

		BTL	CO
1.	Explain the types of micro operations?	**2**	**2**
2.	Compare CO and CA?	**2**	**1**
3.	List the names of Registers?	**2**	**1**
4.	Define Control Word?	**1**	**2**
5.	Explain Complements with Examples?	**1**	**3**

PART-B 3 x5 M = 15 M

		BTL	CO
6.	Define Register Transfer language? Explain the implementation of common bus system using multiplexers.	**3**	**1**
	or		
7.	Illustrate the functioning of micro programmed control unit?	**4**	**2**
8.	Explain Instruction formats and Instruction Types with an example.	**4**	**1**
	or		

9.	Explain about different types of Addressing modes?	**1**	**2**
10.	Design and Explain with suitable example, 4-bit Adder/Subtractor?	**3**	**1**
	or		
11.	Write about functional units with diagram?	**1**	**2**

SCHEME OF EVALUATION

PART-A

SNO	THEORY	MARKS	TOTAL
1	Explain the types of micro operations?	**2**	**2**
2	Compare CO and CA?	**2**	**2**
3	List the names of Registers?	**2**	**2**
4	Define Control Word?	**2**	**2**
5	Explain Complements with Examples?	**2**	**2**

PART-B

SNO	THEORY	MARKS	TOTAL
6	Define Register Transfer language? Explain the implementation of common bus system using multiplexers.	**5**	**5**
7	Illustrate the functioning of micro programmed control unit?	**5**	**5**
8	Explain Instruction formats and Instruction Types with an example.	**5**	**5**
9	Explain about different types of Addressing modes?	**5**	**5**
10	Design and Explain with suitable example, 4-bit Adder/Subtractor?	**5**	**5**
11	Write about functional units with diagram?	**5**	**5**

CMR ENGINEERING COLLEGE
UGC AUTONOMOUS
(Approved by AICTE - New Delhi. Affiliated to JNTUH and Accredited by NAAC & NBA)
Kandlakoya (V), Medchal (M), Medchal - Malkajgiri (D)-501401

MID-II QUESTIONS
COMPUTER ORGANIZATION

II - B.TECH- I-SEM -II MID EXAMINATIONS

Date: 07-01-23 **Time: 10:00AM to 11:30AM**

Subject: COA Branch: CSE, AI&ML, IT, CS
Max. Marks: 25 M

Note: Question paper contains two parts, Part - A and Part - B.
Part-A is compulsory which carries 10 marks. Answer all questions in part-A.
Part-B consists of (2.5) units. Answer any one full question from each unit.
Each question carries 5 marks.

PART-A

5x2=10

1) Define cache hit, cache miss and hit ratio? (CO3)
2) What is Handshaking mechanism? (CO4)
3) What is content addressable memory? (CO3)
4) Write about parallel priority interrupts. (C04)
5) Define delayed load and delayed branch. (C05)

PART-B

3X5=15

6) Explain the Booth's algorithm for multiplication of signed two's Complement numbers (CO5)

OR

7) Design and explain 4-bit adder-sub tractor and 4-bit arithmetic circuit to perform Addition and subtraction using full adders. (CO3)

What are the different modes of data transfer? Explain each mode in detail? (C03)

OR

8) Explain the cache memory mapping techniques. (CO4)

9) E

xplain about vector processing and array processor in detail? (C05)

OR

10) What is pipelining? Name the two pipeline organizations.

Explain about the Arithmetic pipeline with the help of an example. (CO5)

Scheme of Evaluation

Branch: CSE
Year: II-I
Total marks: 10

Answer Any Two Questions

SET-I

Scheme of Evaluation

S.No.	THEORY	MARKS	TOTAL
1	Draw the bus system for four registers and explain	5	5
2	Convert the following numbers with the indicated bases to decimal: $(213201)_4$, $(4310)_5$, and $(1698)_{11}$	5	5
3	What do you understand by Instruction format? How many of its type and how that can be applicable to solve an arithmetic expression X=(A+B)*(C-D).	5	5
4	An 8-bit register contains the binary value 1001011101. What is the register value after an Arithmetic Shift Right? Starting from the initial number 10011100, determine the register	5	5

	value after arithmetic Shift Left, and state whether there is an overflow occur, if yes how it is determine.		

MID – II SET-1

1) **Explain I/O interface?(CO4)**
2) **Write about asynchronous data transfer?(CO4)**
3) **Discuss about a) Auxiliary memory**
4) **Associate memory (CO4)**
5) **Define pipeline? and explain pipeline types?(CO5)**

Branch: CSE
Year: II-I
Total marks: 10

Answer Any Two Questions

SET-I
Scheme of Evaluation

S.No.	THEORY	MARKS	TOTAL
1	Explain I/O interface	5	5
2	Write about asynchronous data transfer	5	5
3	Associate memory	5	5
4	Define pipeline and explain pipeline types	5	5

10. Mapping of COs with POs and PSOs

1 – Slightly 2 – Moderately 3 – Substantive

Course Outcomes (CO)	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO 1	PSO 2
1	1	-	1	-	-	-	-	-	-	-	-	-	1	-
2	1	1	3	1	2	-	-	-	-	-	-	1	-	1
3	-	-	1	1	1	-	-	-	-	-	-	-	-	-
4	1	3	2	2	2	1	-	-	-	-	-	1	-	2
5	1	1	2	3	1	-	-	-	-	-	-	-	2	-
6	1	1	2	1	3	1	1	-	-	-	-	-	-	-
	1	**1**	**2**	**1**	**0**	**-**	**-**	**-**	**-**	**-**	**-**	**0**		

11. Cos,Pos,PSOs Justifications

12. Attainment of Cos,POs and PSOs (Excel Sheet)

13. University Question Papers/ Question Bank

Code No: 134AK

R16

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year II Semester Examinations, April - 2018

COMPUTER ORGANIZATION

(Common to CSE, IT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a)	Explain RTL and its control function.	[2]
b)	Compare horizontal and vertical organization.	[3]
c)	Differentiate jump and loop instructions.	[2]
d)	Briefly explain special processor activities.	[3]
e)	What is an assembler?	[2]
f)	Explain the machine code for: LES DI,[0600H] and NEG 50[BP].	[3]
g)	Explain overflow and underflow.	[2]
h)	Differentiate isolated I/O and memory mapped I/O.	[3]
i)	Explain the cache incoherence.	[2]
j)	Explain the locality of reference.	[3]

PART-B

(50 Marks)

2.a) List and explain different performance measures used to represent a computer system performance.

b) Elucidate the functioning of a Micro program sequencer. [5+5]

OR

3.a) Elucidate common bus system.

b) Formulate a mapping procedure that provides eight consecutive micro instructions for each routine. The operation code has 7 bits and control memory has 4096 words. [5+5]

4.a) Explain the register organization in 8086.

b) Elucidate machine language instruction formats. [5+5]

OR

5.a) Explain the pin configuration details of 8086.

b) Explain the assembler directives with examples. [5+5]

6.a) Explain the steps involved in writing a program using an assembler.

b) Write a program to find out the number of positive numbers and negative numbers from a given series of signed numbers. [5+5]

OR

7.a) Add the contents of the memory location 4000H:0600H to contents of 5000H:0700H and store the result in 8000H:0900H

b) Write a program for addition of two numbers. [5+5]

8.a) Draw a flow chart for Floating point Add/subtract operations.

b) Illustrate asynchronous communication interface in detail. [5+5]

OR

9.a) Explain in detail with neat sketch Booth Multiplication Algorithm.

b) Explain different types of modes of control. [5+5]

10.a) Explain arithmetic pipeline with example.

b) Elucidate Inter processor communication. [5+5]

OR

11.a) Elucidate array processor in detail.

b) Explain various Interconnection Structures. [5+5]

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Code No: 134AK **R16**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, December - 2018
COMPUTER ORGANIZATION
(Common to CSE, IT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a) Write the generic Instruction types present in a computer system. [2]
b) What is the difference between a direct and an indirect address instruction? [3]
c) List the four basic functions of the CPU. [2]
d) Give a note on Instruction Set of 8086. [3]
e) What is an interrupt service routine in microprocessor? [2]
f) How a clock signal is generated in 8086 microprocessor? [3]
g) List four peripherals devices that produce an acceptable output for a person to understand. [2]
h) How many characters per second can be transmitted over a 1200 baud line in Synchronous serial transmission? [3]
i) What are the difficulties that cause the instruction pipeline to deviate from its normal operation? [2]
j) Draw the structure of general purpose multicomputer. [3]

PART - B

5 × 10 marks = 50

2.a) How many references to memory are needed for each type of instruction to bring an operand into a processor register? Explain.
b) With the help of a block diagram, explain how do we select the address of control memory. [5+5]

OR

3.a) Give a brief note on instruction cycle.
b) List and explain the functional units of a computer. [5+5]

4. Draw and explain the 8086 Processor Architecture. [10]

OR

5.a) Explain the Assembler Directives.
b) Discuss the Physical memory organization. [5+5]

6. How to pass parameters to procedures in 8086? Explain in detail with an ALP. [10]

OR

7.a) Is 'c' an assembly language? Justify your answer.
b) With an assembly language program explain stack organization in 8086. [4+6]

8. Compare interrupt driven data transfer scheme with DMA. Using block diagram explain interrupt driven transfer scheme. [10]

OR

9. Explain Booths multiplication algorithm with example. [10]

10.a) Distinguish between the virtual memory and cache memory. Write the merits and demerits of virtual memory.

b) Give a neat sketch that illustrates the components in a typical memory hierarchy. [5+5]

OR

11.a) With the help of a neat diagram explain the match logic for one word of associative memory.

b) What are the various forms available for establishing an interconnection network in a multi processor system? [5+5]

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Code No: 124CN **R15**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, May - 2017
COMPUTER ORGANIZATION
(Computer Science and Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a)	Define the effective address.	[2]
b)	Explain about Logical and Bit Manipulation Instructions.	[3]
c)	Explain about the purpose of Input-output interface.	[2]
d)	Explain about the two-wire control.	[3]
e)	Explain about auxiliary memory.	[2]
f)	What is a bootstrap loader? Explain about the functions of bootstrap loader.	[3]
g)	Explain about the purpose of Bus High Enable pin in 8086.	[2]
h)	Explain about condition code flag register in 8086.	[3]
i)	Explain about One-byte instruction in 8086.	[2]
j)	Explain about FAR PTR and NEAR PTR assembler directive.	[3]

PART-B

(50 Marks)

2. Write a program to evaluate the arithmetic statement:

$$\frac{X-A-B+C*(D*E-F)}{G+H*K}$$

a) Using a general register computer with three address instructions.
b) Using a general register computer with two address instructions. [5+5]

OR

3.a) Explain about the functions of CPU.
b) Explain about Program Control Instructions. [5+5]

4.a) Explain about Source-initiated transfer using handshaking and Destination-initiated transfer using handshaking with a neat diagram.
b) A CPU with a 20-MHz clock is connected to a memory unit whose access time is 40 ns. Formulate a read and write timing diagrams using a READ strobe and a WRITE strobe. Include the address in the timing diagram. [5+5]

OR

5.a) What is the difference between isolated I/O and memory-mapped I/O? What are the advantages and disadvantages of each?
b) Explain about Intel 8089 IOP. [5+5]

6. A computer uses RAM chips of 1024 × 1 capacity.
a) How many chips are needed, and how should their address lines be connected to provide a memory capacity of 1024 bytes?
b) How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus. [5+5]

OR

7.a) Obtain the Boolean function for the match logic of one word in an associative memory taking into consideration a tag bit that indicates whether the word is active or inactive.
b) Explain about Virtual Memory with the implementation details. [5+5]

8.a) Explain about the register organization of 8086.
b) Explain about the concept of segmented memory with a neat diagram. Explain its advantages. [5+5]

OR

9.a) Explain about addressing modes of 8086.
b) Explain about the functions of opcode prefetch queue in an 8086 system. [5+5]

10.a) Explain about different instruction formats in 8086.
b) Write an Assembly Language program to perform one byte BCD addition. [5+5]

OR

11.a) Explain about different types of Assembler directives and operators.
b) Write an ALP program to find transpose of a 3×3 matrix. [5+5]

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Code No: 124CN

R15

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year II Semester Examinations, December - 2017
COMPUTER ORGANIZATION
(Computer Science and Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) Give an example each of Zero-address, One-address, two-address and three-address instruction. [2]
b) Write a program that can evaluate the expression A * B + C * D, in a single-accumulator processor. Assume that the processor has Load, store, Multiply, and Add instructions and that all values fit in the accumulator. [3]
c) What is the basic advantage of using interrupt-initiated data transfer over transfer under program control without an interrupt? [2]
d) What are the functions of typical I/O interface? [3]
e) Explain the terms Hit Ratio and Miss ratio. [2]
f) How many 128 × 8 RAM chips are needed to provide a memory capacity of 2048 bytes? How many lines of address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips? [3]
g) In Intel microprocessor what is meant by segment register? [2]
h) What are the functions of flag registers in 8086 microprocessor? [3]
i) List few branch and call instructions. [2]
j) What are assembler directives? [3]

PART-B

(50 Marks)

2.a) Explain different functional units of a digital computer.
b) Mention the four types of operations to be performed by an instruction in a computer. What are the basic types of instruction formats? Give examples. [5+5]

OR

3.a) What is an interrupt? What are the uses of interrupts? Explain about the different type of interrupts?
b) What is an addressing mode? List the different types of addressing modes. Explain index addressing mode with example program. [5+5]

4.a) A CPU with a 20-MHz clock is connected to a memory unit whose access time is 40 ns. Formulate a read and write timing diagram using a READ strobe and a WRITE strobe. Include the address in the timing diagram.
b) Describe in detail about IOP organization. [4+6]

OR

5.a) Describe the data transfer method using DMA.
b) Why are the read and write control lines in a DMA controller bi-directional? Under what condition and for what purpose are they used as inputs? Under what condition and for what purpose they used as outputs? [5+5]

6.a) Consider a processor running a program. 30% of the instructions of which require a memory read or write operation if the cache bit ratio is 0.95 for instructions and 0.9 for data. When a cache bit occurs for instruction or for data, only one clock is needed while the cache miss penalty is 17 clocks to read/write on the main memory. Work out the time saved by using the cache, given the total number of instructions executed is 1 million.

b) Explain in detail about associative mapping technique. [4+6]

OR

7.a) A magnetic disk system has the following parameters:
T_s = average time to position the magnetic head over a track
R = rotation speed of disk in revolutions per second
N_t = number of bits per track
N_s = number of bits per sector
Calculate the average time T_a that it will take to read bits per inch?

b) Explain in detail about virtual memory. [4+6]

8.a) What is pipelining? What are its principles?

b) Describe with examples how a 20 bit physical address of an instruction is generated in 8086 microprocessor? Explain the functions of following pins in 8086 microprocessor:
i) NMI
ii) DEN
iii) QS_0 - QS_1. [5+5]

OR

9.a) Write the special functions of general purpose registers.

b) Register R5 is used in a program to point to the top of a stack. Write a sequence of instructions using the Index, Autoincrement, and Autodecrement addressing modes to perform each of the following tasks:
i) Pop the top two items of the stack, add them, and then push the result onto the stack.
ii) Copy the fifth item from the top into register R3.
iii) Remove the top ten items from the stack. [4+6]

10. Write an ALP for sorting Ascending and Descending order of a series. [10]

OR

11. Describe with the neat diagram the architecture of 8086 Microprocessor. [10]

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14. Power point presentations (PPTs)

Unit no	Topic name	Link
1	Instruction code	https://www.youtube.com/watch?v=mEw09EJwj30
1	Instruction cycle	https://www.youtube.com/watch?v=SFsnysyVhzA
1	Microprogrammed control unit	https://www.youtube.com/watch?v=81v7JqLbTMI http://www.infocobuild.com/education/audio-video-courses/computer-science/ComputerOrganization-IIT-Madras/lecture-07.html
2	Architecture of 8086	https://www.youtube.com/watch?v=CEL-jT4qFCk
2	Addressing modes of 8086	https://www.youtube.com/watch?v=hVRtfcvt1ns
2	Instruction set of 8086	https://www.youtube.com/watch?v=V3AeSmlZzw8
3	Interrupts of 8086	https://www.youtube.com/watch?v=LUVJxy-pGlM
3	Procedures and macros	https://www.youtube.com/watch?v=ybz0MYyum5M
3	Stack structure of 8086	https://www.youtube.com/watch?v=t35b-8w4Yrg
4	Computer arthimatic (addition , substraction)	https://www.youtube.com/watch?v=o-WXqnagg0c
4	Floating point arthimatic (addition)	https://www.youtube.com/watch?v=KiWz-mGFqHI
4	Asynchronous data transfer	https://www.youtube.com/watch?v=EzEqUH93C4U
5	Memory organization	https://www.youtube.com/watch?v=z_dSASDYc6c
5	Pipelining	https://www.youtube.com/watch?v=hGjX1Iw9Qxw
5	Multiprocessors	https://www.youtube.com/watch?v=fG3pmE2iRzo

15. Websites/URLs/ e- Resources

- www.wiley.com
- www.faadooengineers.com
- www.scribd.com
- www.slideshare.net
- www.google.com/co
- www.bookadda.com
- http://www.infocobuild.com