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Department of Electronics and Communication Engineering

Logisim-evolution Simulator Tool

Digital Design Innovation: Logisim-evolution Virtual Lab Experiment

Overview

Our laboratory facilities are enhanced by **Logisim-evolution**, a state-of-the-art graphical tool for designing and simulating digital logic circuits. While physical hardware is essential, Logisim-evolution provides students with a "virtual sandbox" to prototype complex digital systems—ranging from simple logic gates to fully functional 32-bit CPUs—before moving to physical implementation.

Why Logisim-evolution?

Logisim-evolution is an advanced "evolutionary" branch of the original Logisim, featuring professional-grade tools that prepare students for industry-standard EDA (Electronic Design Automation) software.

Key Features & Capabilities:

- **Chronogram (Timing Diagrams):** Allows students to observe signal propagation delays and race conditions in real-time.
- **FPGA Integration:** Seamlessly converts graphical "drawn" circuits into **VHDL or Verilog** code, which can be downloaded directly to our **Nexys 4 Artix-7 FPGA** boards.
- **Large-Scale Components:** Includes built-in libraries for 64-bit RAM/ROM, ALUs, and complex I/O devices (Keyboards, Hex Displays, Joysticks).
- **Educational SoC Design:** Features a specialized "Electronics" library and support for building and testing custom microprocessors.

Integrated Curriculum Applications

Students utilize Logisim-evolution across multiple semesters to master digital architecture:

1. **Combinational Logic:** Building decoders, multiplexers, and arithmetic units (Adders/Subtractors).

2. **Sequential Systems:** Designing Finite State Machines (FSMs), registers, and synchronous counters.
3. **CPU Architecture:** Designing a "Toy CPU" to understand how the Fetch-Decode-Execute cycle works at the gate level.
4. **Hardware Description Language (HDL) Bridge:** Learning how graphical logic translates into structural VHDL code.

The "Sim-to-Silicon" Workflow

Our lab follows a professional design flow:

1. **Design:** Draw the circuit in the Logisim-evolution GUI.
2. **Verify:** Use the **Chronogram** to ensure timing and logic are correct.
3. **Synthesize:** Use the software's built-in tool to generate HDL code.
4. **Implement:** Deploy the design onto the **Artix-7 FPGA** for real-world testing.

Student Resources

> **Get Started:** Logisim-evolution is available on all lab workstations. Students are encouraged to download the portable version for their personal laptops to continue their projects at home.

- **Software Version:** v3.8.0 (or your specific version)
- **Platform:** Windows/Linux/MacOS (Java-based)
- **Documentation:** Access the "Logisim-evolution User Guide" and "Digital Logic Lab Manual" via the college Intranet.

Laboratory Advantages

- **Zero-Risk Environment:** Students can experiment with complex wiring without the risk of damaging physical components or ICs.
- **Visual Learning:** The color-coded wires (Dark Green = Low, Bright Green = High, Blue = Unknown) provide instant visual feedback on circuit behavior.
- **Complex Debugging:** Features like "Logging" and "Step-by-Step Simulation" allow students to pause time and find bugs in their logic.