Nexys 4 DDR Artix-7 FPGA Trainer Board

Facility Spotlight: Advanced Digital System Design Lab Experimets(Nexys 4 Artix-7)

Overview

Our laboratory is now equipped with the **Digilent Nexys 4 DDR Artix-7 FPGA Trainer Board**. Unlike traditional microcontrollers that execute software instructions, FPGAs allow students to design **hardware-level circuitry**. The Nexys 4 is a complete, ready-to-use digital circuit development platform based on the high-performance Xilinx Artix-7™ FPGA, designed to bring industry-grade applications into the classroom.

Core Technical Specifications

At the heart of the board is the **Xilinx XC7A100T-1CSG324C** FPGA, offering massive resources for complex logic designs:

- **Logic Capacity:** 101,440 logic cells (15,850 logic slices, each with four 6-input LUTs and 8 flip-flops).
- **Memory:** 4,860 Kbits of fast block RAM and **128 MiB DDR2 SDRAM** for large data buffers.
- **DSP Power:** 240 DSP slices for high-speed arithmetic and signal processing.
- **Clocking:** Six clock management tiles, each with a Phase-Locked Loop (PLL) for precise internal clock control exceeding 450 MHz.
- **Analog Integration:** On-chip Analog-to-Digital Converter (XADC).

Integrated Peripherals & Interfaces

The Nexys 4 is "industry-in-a-box," featuring a wealth of on-board I/O that eliminates the need for external components in most projects:

- **Visual Output:** 12-bit VGA output (4096 colors) and two 4-digit 7-segment displays.
- **Sensors:** 3-axis accelerometer (ADXL362) and a high-accuracy temperature sensor (ADT7420).
- **Audio:** PDM MEMS microphone and a Mono PWM audio output (speaker amplifier).

- **Connectivity:** 10/100 Ethernet PHY, USB-UART Bridge, and a USB HID Host for keyboards/mice.
- **User I/O:** 16 slide switches, 16 user LEDs, 2 tri-color (RGB) LEDs, and 5 pushbuttons.
- **Expansion:** Five Pmod™ ports (four standard and one for XADC signals) for adding custom modules.

Educational Objectives & Curriculum

By working with the Nexys 4, students transition from simple logic gates to sophisticated system-on-chip (SoC) architectures:

1. **Digital Logic Fundamentals:** Designing adders, multiplexers, and state machines using **Verilog** or **VHDL**.
2. **Embedded Processor Design:** Implementing "soft" microprocessors like **Xilinx MicroBlaze** directly on the FPGA fabric.
3. **VGA Controller Development:** Learning how to generate video timing signals to display graphics on monitors.
4. **Hardware-Software Co-Design:** Utilizing the **Xilinx Vivado Design Suite** for synthesis, implementation, and real-time debugging.

Student Guidelines for Lab Usage

> **Important:** FPGA boards are sensitive to Electrostatic Discharge (ESD). Students must use antistatic wrist straps and handle boards by the edges only.

Standard Lab Workflow:

1. **Code:** Write hardware description code (Verilog/VHDL) in **Vivado**.
2. **Simulate:** Verify logic timing using the Vivado Simulator.
3. **Synthesize:** Translate code into a hardware bitstream.
4. **Program:** Upload the bitstream via the onboard USB-JTAG port.